TRANSIENT ANALYSIS OF MESFET AMPLIFIERS FOR SUBNANO-SECOND PULSE OPERATION

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in Partial Fulfilment of the Requirements
for the Degree of
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By
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to the
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AUGUST, 1978

CERTIFICATE

This is to certify that the work on TRANSIENT ANALYSIS OF MESFET AMPLIFIERS FOR SUBNANOSECOND PULSE OPERATION has been carried out under our supervision and this has not been submitted elsewhere for a degree.

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ABSTRACT

Transient analysis of MESFET amplifier in common source and source follower configuration has been carried out by state variable method. The amplifier are connected to source and load by transmission lines. Characteristic equation method for solving hyperbolic partial differential equation is used for numerical solution of transmission line equation. The effect of circuit and device parameters on the operation of these circuits has been studied for 20 picosecond triangular pulses.

One of the significant results achieved here is the realization of the fact that there is substantial reflection of the incident pulse at the input terminals. It is observed that low input impedance line (e.g. 10 ohms) is preferable for common source amplifiers. Active loads help to get a better rise and fall time of output pulse. It is desirable to use a MESFET of low gate to source capacitance for source follower circuit. The gate contact resistance has an insignificant effect on transmitted pulses in all the circuits analysed. In trinsic transistor delay has its effect only on the transmitted pulse.

ACKNOWLEDGEMENT

I am grateful to my thesis supervisors Professor K.C. Gupta and Dr. M.M. Hasan for their help, timely advice and excellent understanding throughout the preparation of this work. Among many other things, I particularly wish to thank Professor Gupta for giving me an introduction to research, where often seemingly difficult problems turn out to be absurdly simple and the so-called obvious ones immensely difficult. I really enjoyed doing my thesis.

A thesis while supposedly the work of an individual is actually a product of diverse influences both covert and overt. I owe to my friends much more than a few words of thanks for their helpful discussions and encouragements in many ways. I am astonished at the speed and accuracy of Mr. C.M. Abraham who typed this thesis. I also wish to thank Mr. V.P. Gupta whose nimble fingures produced immaculate drawings.

List of Contents

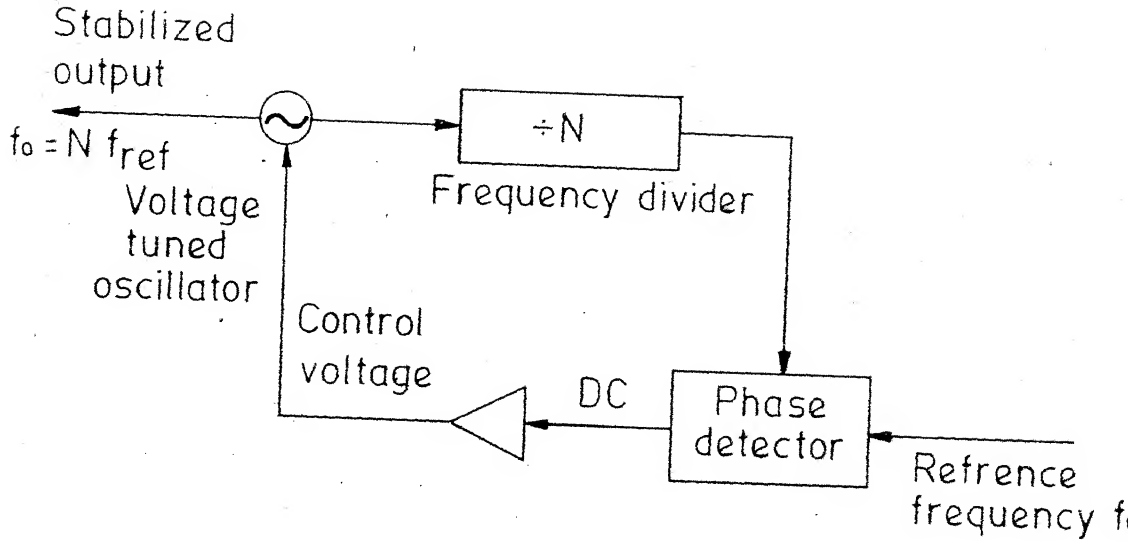
Chapter 1

INTRODUCTION

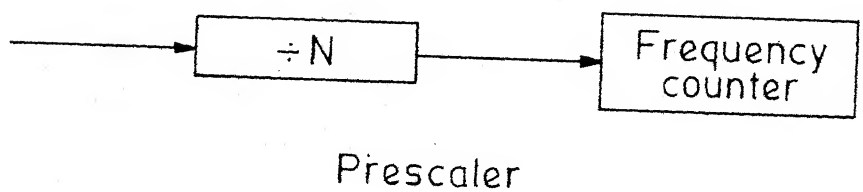
GaAs MESFET logic[1] circuit has the potentiality of operating at giga-bit rates. A transmission line ring circuit with two MESFET around the ring[2] is proposed for generation of subnanosecond pulses. The major contribution of high-speed GaAs MESFET logic is likely to be the extension of RF digital signal processing into the microwave-frequency range. Many tasks that are presently performed with complex and cumbersome microwave techniques could be implemented with relatively simple monolithic chips, assuming that an integration level of sufficient complexity can be achieved. Presently high speed GaAs MESFET logic can implement a number of basic medium-complexity functions at frequency upto 3 GHz. Envisioned improvements could double this speed.

Figure 1.1 shows several typical applications in block-diagram form. Stabilization and frequency control of microwave signal sources using phase-locked loops is a popular technique. Realization of the divide-by-N function with GaAs MESFET digital frequency divider would extend this technique to the divider's highest frequency.

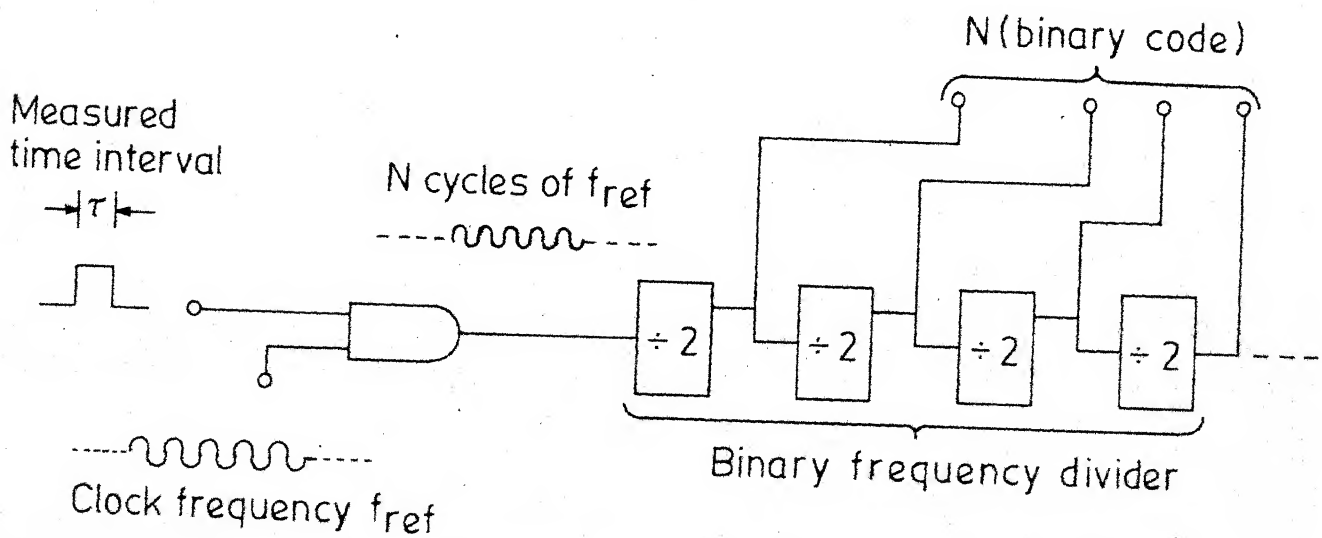
One of the problems with a high speed logic circuit is the interconnections which behave like transmission lines (e.g. if a 20 ps pulse is taken the wavelength



Frequency synthesizer and stabilized frequency source.



Prescaler



Period and time interval measurement.

Fig. 1.1 - MESFET logic has a number of microwave - frequency applications, including frequency synthesizer, prescalers and time interval measurements. Each of these have, in common, a frequency divider, which can be implemented readily with MESFET logic.

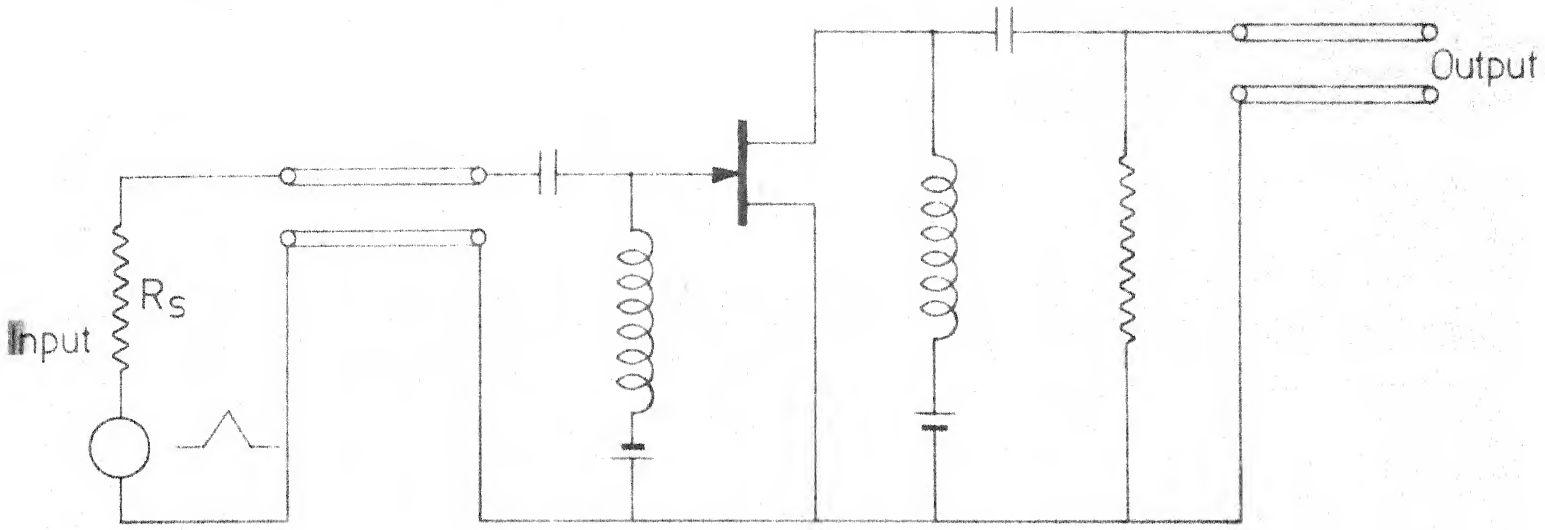


Fig. 1.2(a)

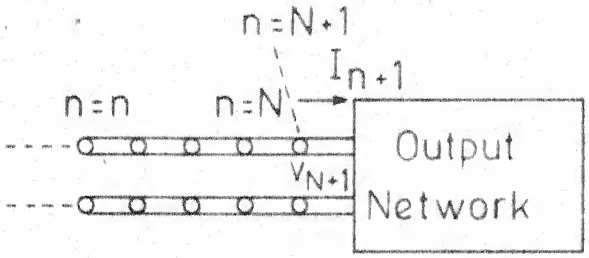


Fig. 1.2(b)

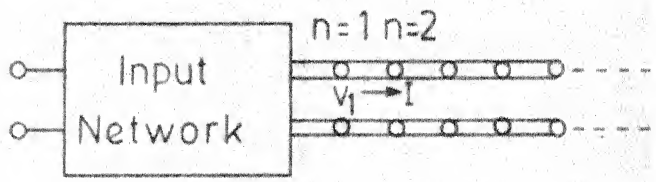


Fig. 1.2(c)

Fig. 1.2 - MESFET common source pulse amplifier with input and output transmission line and its equivalent representation.

involved is 1.2 cm). So the whole circuit can be posed as a problem of transmission line with an active load at the input or at the output as shown in Fig. 1.2. The characteristic of the load impedance is that it is a function of the input voltage.

Lossless transmission lines can be represented by hyperbolic partial differential equations and the boundary condition is a function of the input voltage. Therefore, a closed form solution of the problem appear in a complicated form. The present study is aimed at an approximate numerical solution of this type of circuit with active device in different configurations. Also it is attempted to find out the dependence of the transmitted and reflected pulses changes with change in circuit parameters.

Suitable models for transient analysis of MESFET at different circuit configurations and the transient analysis of transmission lines have been developed and discussed in Chapter 2 and Chapter 3 respectively.

Effects of variations in various circuit parameters have been studied in Chapter 4, Chapter 5 and Chapter 6. Results of this study are used to develop a circuit configuration suitable for amplification of narrow pulses. Lumped elements used only for biasing of MESFET are not critical in circuit design.

Chapter 2

MESFET AND ITS EQUIVALENT CIRCUIT

2.1 MESFET

Mainly because of high electron mobility of GaAs and therefore its promise of high frequency performance a number of investigators have used n-type GaAs as the channel material of FETs. A typical value of electron mobility[3] in GaAs is 7000 $cm^2/v\text{-}sec.$, an increase of more than a factor of five over silicon.

Difficulty with diffused[3,4] gate is that controlled diffusion of impurities in GaAs has not presently advanced to the point where it is possible to meet the fine geometrical requirements in the gate. In addition irreversible changes can occur in GaAs at the high temperature usually necessary for diffusion process.

It is well known that the 'free' surface[3] of both silicon and GaAs contains high density of surface charge which diminishes the penetration of the field into the bulk. It is also well established that when a layer of silicon dioxide is placed over the silicon surface, the chargeable surface state density is drastically reduced. This makes the insulated gate FET a practical device for this material.

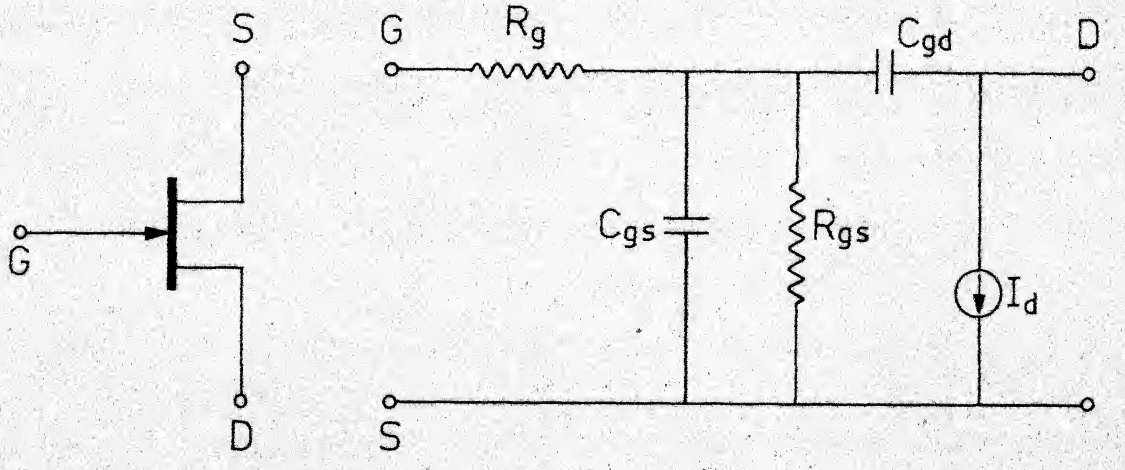


Fig. 2.1 - Equivalent circuit of the MESFET.

A similar reduction in surface state density has not been observed in GaAs insulated gate FET, with the result that the gate is relatively inefficient in modulating the channel conductance. Because of these problems both insulated gate and diffused gate are unfavourable for GaAs FET[3].

A FET structure which is not faced with the problem described above and which has a number of desirable feature has been proposed by Mead[5]. The undesirable effects produced by surface states in the insulated gate FET are avoided by Mead's device by making these states working part of a metal-semiconductor junction or schottky barrier. In this case, the effect of large surface charge density is to fix (approximately) the electrostatic potential at the semiconductor surface with respect to the metal Fermi level. Thus, when the metal electrode is used as gate, a negative charge applied to the gate extends the depletion region into the n-type substrate and corresponding potential drop appears entirely across the semiconductor.

2.2 Equivalent Circuit

An equivalent circuit of a MESFET used for present analysis is shown in Fig. 2.1. Here R_g represents the series resistance associated with the gate to source schottky barrier diode and the gate contact. A typical value of R_g is 1 to 10 ohms[4]. The parallel combination of

C_{gs} and R_{gs} respresents the schottky barrier gate to source diode. Values of C_{gs} and R_{gs} depend on gate-to-source voltage V_g. The capacitance C_{gs} may be represented by

$$C_{gs} = C_o/\sqrt{1 - V_g/V_b} \qquad (2.1)$$

where C_o is the junction capacitance for zero bias and is typically 0.2 to 0.5 pF. V_b is the built-in voltage which has a typical value of 0.1 to 0.3 volt for a good GaAs schottky barrier junction. It may be noted that the value of C_{gs} rises sharply for V_{gs} greater than zero and becomes infinitely large for V_g equal to V_b. This nonlinearity in input capacitance plays a significant role in MESFET circuits for narrow pulses. It may be noted that the gate voltage V_g can not exceed V_b because of infinitely large value of junction capacitance for V_g equal to V_b.

The junction resistance[6] R_{gs} may be evaluated as

$$R_{gs} = (V_b - V_g)/\left\{I_s[\exp q(V_g - V_b)/nKT - 1]\right\} \qquad (2.2)$$

where I_s is the reverse saturation current of the diode and is of the order of a nanoampere. The factor q/KT has a value of 38.7 at 300°K where q represents the value of electronic charge, K is the Boltz-man's constant and T is the operating temperature in degree-Kelvin. The above relation for R_{gs} becomes indeterminate for V_g equal to V_b, in which case the value of R_{gs} may be found as

$$R_{gs} = KT/qI_s$$

For $I_s = 10^{-9}$ A and T = 300°K. This relation yields, the value of R_{gs} equal to 25.9 x 10^6 ohms. It may be noted that even for V_g equal to V_b where the capacitance reactance of the diode tends to zero, the value of R_{gs} is fairly large. Thus for narrow pulses the diode clamping is provided by the non-linear capacitance rather than by the non-linear resistance (which is the case at lower frequencies).

Drain to gate feed-back capacitance is taken as a constant value of the order of 0.02 pF. In actual circuit this capacitance never varies more than 15 percent.

The drain current source I_d is a function of gate voltage V_g and the drain voltage V_d. When the MESFET is operating in the pinch-off regions, i.e., when the quantity $(V_d - V_g + V_b)$ is greater than the pinch-off voltage V_p, the drain current I_d becomes a function of gate voltage alone. On the basis of analysis of FETs discussed by Sze[6,7] one can write for $(V_d - V_g + V_b) > V_p$

$$I_d = I_{sat}\left[1 - 3\left(\frac{V_b - V_g}{V_p}\right) + 2\left(\frac{V_b - V_g}{V_p}\right)^{1.5}\right] \qquad (2.4)$$

Where I_{sat} represent saturation current for V_g equal to V_b. The two constants I_{sat} and V_b in the above equation may be evaluated from d.c. characteristics of MESFET used in the circuit. For this purpose, values of I_d for only two

different values of V_g in the pinch-off region are sufficient. For $(V_d - V_g + V_b) < V_p$ the drain current may be expressed as

$$I_d = A[V_d - B[(V_d - V_g + V_b)^{3/2} - (V_b - V_g)^{3/2}]] \qquad (2.5)$$

Where A and B are two constants that depend on the physical parameters of the MESFET. These constants can be determined from the characteristics of the MESFET in triode region. Again two measured values of I_d are sufficient for evaluation of these parameters. To match the characteristic curves of the two region with a very high accuracy, for a particularly defined I_{sat} and V_b, a subroutine has been developed (see Appendix I) to find the values of A and B.

Another characteristic of the equivalent circuit of MESFET (not indicated in Fig. 2.1) is the intrinsic delay in the transmission of signal through MESFET. This is supposed caused by transit time of the carrier in the channel and is incorporated in the model as a delay between V_g and the drain current I_d produced by this voltage. It can be expressed as

$$I_d(t) = f\{V_g(t - \tau), \quad V_d(t - \tau)\} \qquad (2.6)$$

Typical value of delay τ ranges from 2.5 to 7.5 ps.

Chapter 3

TRANSIENT ANALYSIS OF TRANSMISSION LINE

The procedure for transient analysis of transmission lines employed here is based on the method of characteristics used for numerical solution of hyperbolic partial differential equations. In this report this method has been used for uniform transmission lines[8,9] but can also be extended for non-uniform transmission lines[10]. The present analysis however, does not take microstrip dispersion into account. Since the transmission line lengths used in the circuit are small, it is expected that the dispersion effects will not alter the basic behaviour of the circuit. A more complete analysis however should include the disperse characteristics of the transmission line used.

The set of partial differential equations describing TEM transmission in a lossless line can be written as,

$$-\frac{\partial V}{\partial Z} = L \frac{\partial i}{\partial t} \tag{3.1}$$

$$-\frac{\partial i}{\partial Z} = C \frac{\partial V}{\partial t} \tag{3.2}$$

To review[11,12] the solution of hyperbolic equations, consider now the integration of a single simple first order partial differential equation of the type

$$A \frac{\partial F}{\partial t} + B \frac{\partial F}{\partial Z} = C \tag{3.3}$$

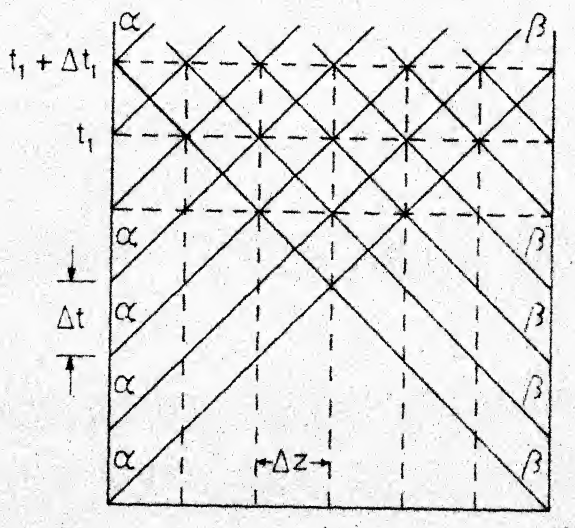


Fig. 3.1 - Families of α and β characteristic curves in the z - t plane for a uniform transmission line (N = 6).

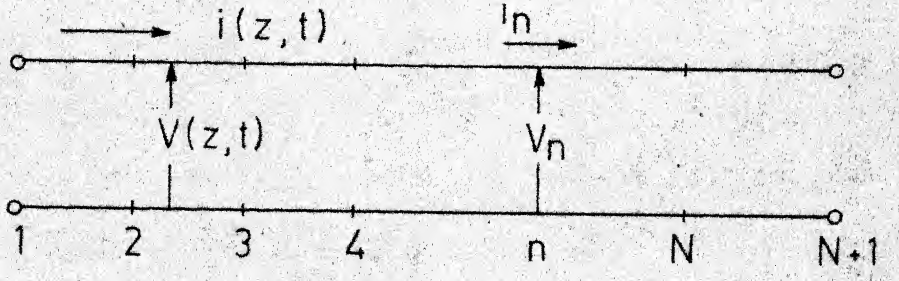


Fig. 3.2 - Division of transmission line in N section for transient analysis.

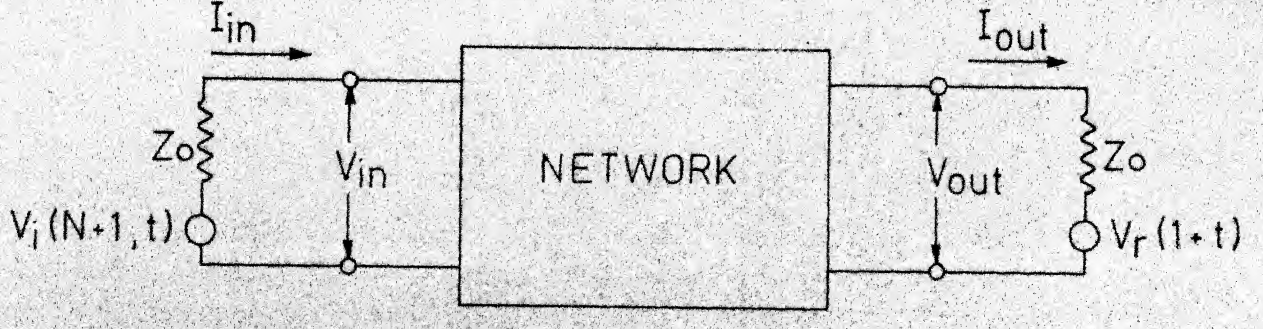


Fig. 3.3 - Equivalent representation of network with transmission line at input and output.

Where A,B and C are functions of t,Z, and F and whose solution is F = F(Z,t). The partial derivative of F along a direction making an angle θ with t-axis is given by simple vector addition, as,

$$\text{Cos } \theta \frac{\partial F}{\partial t} + \text{Sin } \theta \frac{\partial F}{\partial t} \tag{3.4}$$

Therefore, as revealed by comparision with equation (3.3)

$$\tan \theta = \frac{B}{A} = \left(\frac{\partial Z}{\partial t}\right)_c \tag{3.5}$$

where $\left(\frac{dZ}{dt}\right)_c$ represents the slope of the tangent line. The slope $\left(\frac{dZ}{dt}\right)_c$ which is defined at each point in the Z,t plane in terms of B/A is called the characteristic slope. The entire family of characteristic directions form a directive field in the Z,t plane, and the curve that is everywhere tangent to the direction field is known as characteristic curve.

Since,

$$F = F(Z,t)$$

$$dF = \frac{\partial F}{\partial Z} \cdot dZ + \frac{\partial F}{\partial t} \cdot dt.$$

Then, along the characteristic curves,

$$dF = \frac{\partial F}{\partial Z} \, dZ + \frac{\partial F}{\partial t} \cdot \frac{B}{A} \cdot dZ$$

$$= \left(A \frac{\partial F}{\partial Z} + B \frac{\partial F}{\partial t}\right) \frac{dZ}{A} = C \frac{dZ}{A} \tag{3.6}$$

as is shown by introducing equation (3.5) into equation (3.6) consequently

$$\frac{dZ}{A} = \frac{dt}{B} = \frac{dF}{C}$$

along a characteristic curve. Thus, if F at one point along a characteristic curve is known, dF can be calculated for an adjacent point on this curve. Continuing this operation permits F to be established at all points along the characteristic by simple numerical technique.

In the present problem, the two independent partial differential equations (3.1) and (3.2) are to be solved simultaneously. It is to be noted that two distinct characteristic directions are found at each point. To facilitate discussion, the equations (3.1) and (3.2) are rewritten as,

$$L\, i_t + v_z = 0 \qquad (3.1)$$

$$C\, v_t + i_z = 0 \qquad (3.2)$$

where, the subscripts refer to the operation of partial differentiation. Since the entire system of equations has to be solved simultaneously, equations (3.1) and (3.2) are identical with the following equation

$$\lambda_1(L\, i_t + v_z) + \lambda_2(C\, v_t + i_z) = 0 \qquad (3.7)$$

where λ_1 and λ_2 are arbitrarily selected multipliers, when the variables are seperated, equation (3.7) can be rewritten as

$$(\lambda_1 L i_t + \lambda_2 i_z) + (\lambda_2 C v_t + \lambda_1 v_z) = 0$$

To find the characteristic directions along which differentials of i and v are most simply related, the direction tan θ, determined by equation (3.3) has to be the same for the two unknows v and i. Thus,

$$\left(\frac{dZ}{dt}\right)_c = \frac{\lambda_2}{\lambda_1 L} = \frac{\lambda_1}{\lambda_2 C}$$

or,

$$\lambda_1^2 L = \lambda_2^2 C$$

or,

$$\lambda_1 = \lambda_2 \sqrt{L/C}$$

Using these relations, the characteristic directions are given by

$$\frac{dZ}{dt} = \pm \frac{1}{\sqrt{LC}}$$

Families of characteristic curves have members commonly denoted by α and β. These are shown in Fig. 3.1 for a uniform line. Along α curve (forward characteristic)

$$\frac{dZ}{dt} = \frac{1}{\sqrt{LC}} \qquad (3.8)$$

and along β-curve (backward characteristics)

$$\frac{dZ}{dt} = -\frac{1}{\sqrt{LC}} \qquad (3.9)$$

Along these characteristics equations (3.1) and (3.2) may be written as ordinary differential equations. We have,

along α,

$$\frac{d}{dt}\left[v_1(Z,t) + \sqrt{\frac{L}{C}} \cdot i(Z,t)\right] = 0 \qquad (3.10)$$

along β,

$$\frac{d}{dt}\left[v_1(Z,t) - \sqrt{\frac{L}{C}} \cdot i(Z,t)\right] = 0 \qquad (3.11)$$

It may be noted that although equations (3.10) and (3.11) include derivatives only with respect to t, the variables t and Z are related by characteristics (3.8) and (3.9). Thus a change in t has associated with it a change in Z.

Computations are carried out in terms of two voltage variables V_i and V_r defined as

$$V_i = V(Z,t) + \sqrt{L/C}\, i(Z,t) \qquad (3.12)$$

and

$$V_r = V(Z,t) - \sqrt{L/C}\, i(Z,t) \qquad (3.13)$$

It is to be noted that V_i is constant along the forward characteristics (3.8) and V_r is constant along the backward characteristics (3.9).

For numerical computation the length of the transmission line is divided in N sections with equal delays of Δt pico-second (see Fig. 3.2). The time interval Δt is the increment used for the transient analysis of the circuit. The analysis is now carried out by writing 2(N + 1) difference equations in the time domain. These equations are given as,

$$V_i(n,t) = V_i(n-1,\ t-\Delta t),\ n = 2....N \qquad (3.14)$$

and

$$V_r(n,t) = V_r(n+1,\ t-\Delta t),\ n = 1....(N-1) \qquad (3.15)$$

where $V_i(n,t)$ and $V_r(n,t)$ denote the values of the voltage variables at various points along the transmission line at the time instant t. The boundary values $V_i(1,t)$ and $V_r(N+1,t)$ are determined from the properties of the network connected at the input and the output end respectively.

At the input by Kirchoff's Law,

$$V_i(1,t) = V_1(t) + Z_o\, i_1(t) \tag{3.16}$$

and at the output,

$$V_r(N+1,t) = V_{N+1}(t) - Z_o\, i_{N+1}(t) \tag{3.17}$$

Where Z_o is the characteristic impedance of the transmission line ($= \sqrt{L/C}$). Corresponding equivalent circuits are shown in Fig. 1.2(a) and (b) respectively. Voltage and currents at any point along the line may be written as

$$V(Z,t) = (V_i + V_r)/2 \tag{3.18}$$

$$i(Z,t) = \frac{1}{Z_o}(V_i - V_r)/2 \tag{3.19}$$

When the transient analysis of a network (a MESFET circuit, for example) with transmission lines connected at the input and output is being carried out, an equivalent representation shown in Fig. 3.4 may be used. $V_i(N+1, t)$ at the input and $V_r(1,t)$ at the output are known from analysis of the lines connected at the input and the output respectively. Currents $i_{in}(t)$ and $i_{out}(t)$ are calculated from analysis of the network.

$V_r(N+1,t)$ at the input and $V_i(1,t)$ at the output are needed for continuation of transmission line analysis and are found as follows,

$$V_r(N+1,t) = V_i(N+1,t) - 2\, Z_o\, i_{in} \qquad (3.20)$$

and $$V_i(1,t) = V_r(1,t) + 2\, i_{out}\, Z_o \qquad (3.21)$$

Computer program developed for transient analysis of transmission line is given in Appendix 1.

Chapter 4

COMMON SOURCE PULSE AMPLIFIER CONFIGURATION

4.1 Transient Analysis[1]

The equivalent circuit along with biasing network considered for the present analysis is shown in Fig. 4.1. The two transmission lines connected at input and output have characteristic impedance Z_1 and Z_2 respectively. V_i and V_r are two parameters introduced for convenience of transmission line transient analysis and are defined as,

$$V_i = V_{in} + Z_1 I_{in} \qquad (4.1)$$

$$V_r = V_{out} + Z_2 I_{out} \qquad (4.2)$$

where I_{in} and I_{out} are input and output currents and V_{in} and V_{out} are input and output voltages respectively. Sign convention used is positive for currents when flowing from left to right or from top to bottom in all the figures. R_L is a resistor connected across the output to limit the output voltage swings especially when reflection from the transmission line connected at the output terminal is unfavourable. Value of R_L is much higher than the characteristic impedance Z_o of the transmission line, say 500 ohms for a 50 ohms impedance line. All other circuit elements except R_L as shown in the Fig. 4.1 are numbered by subscript 1,2,3, ...n.

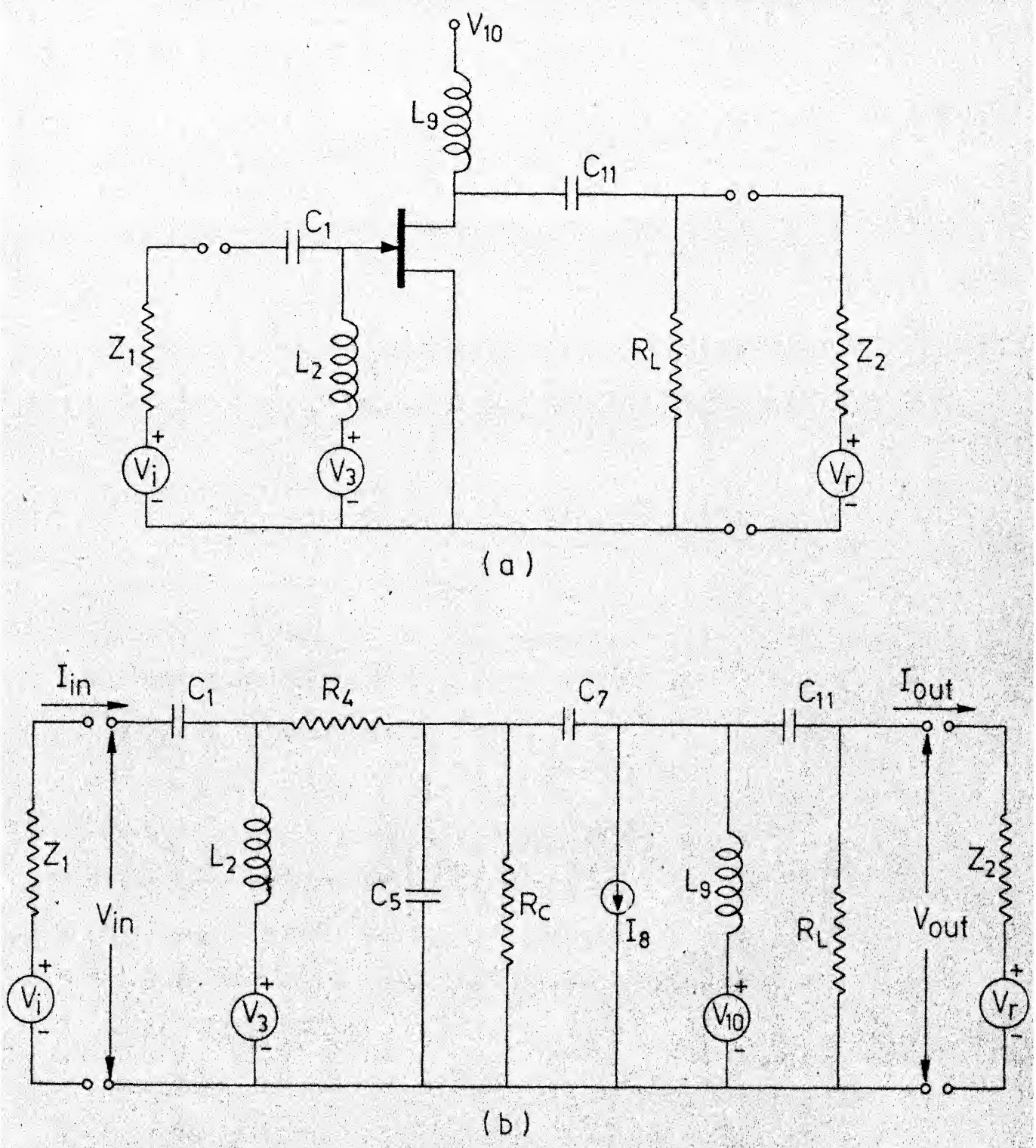


Fig. 4.1 - MESFET in common source configuration with biasing network and input - output transmission line equivalent circuit.

This facilitates nomenclature of currents and voltages associated with these elements. For example I_6 and V_6 represent the current (from top to bottom in Fig. 4.1) and voltage across the sixth element.

The capacitors C_1 and C_{11} block the d.c. voltages from input and output signals. The inductors L_2 and L_9 are used for blocking the R.F. signals from bias sources. Inductors are used instead of resistors because a small value of inductance can provide a very large a.c. impedance in GHz range and can easily be fabricated on a dielectric substrate. MESFET itself is represented by R_4, C_5, R_6, C_7 and I_8 as discussed earlier in Chapter 3.

The transient analysis of the circuit has been carried out by using state variable approach[13]. Voltage across capacitors and the currents in the inductors are taken as state variables. Other voltages and currents required for the analysis are to be expressed in terms of these state variables and its derivatives.

Input and output currents can be expressed in terms of state variables as

$$I_{in} = C_1 \frac{dV_1}{dt} \tag{4.3}$$

$$I_{out} = C_{11} \frac{dV_{11}}{dt} \left(\frac{R_L}{R_L + Z_2}\right) - \frac{V_r}{R_L + Z_2} \tag{4.4}$$

These relations enable V_{in} and V_{out} to be calculated from (4.1) and (4.2) respectively.

Derivatives of the state variables used for finding I_{in}, I_{out} and for updating the values of the state variables are derived by writing circuit equations based on Kirchoff's law. These may be written as

$$\frac{dV_1}{dt} = I_1/C_1 \tag{4.5}$$

$$\frac{dI_2}{dt} = V_2/L_2 \tag{4.6}$$

$$\frac{dV_5}{dt} = I_5/C_5 \tag{4.7}$$

$$\frac{dV_7}{dt} = I_7/C_7 \tag{4.8}$$

$$\frac{dI_9}{dt} = V_9/L_9 \tag{4.9}$$

$$\frac{dV_{11}}{dt} = I_{11}/C_{11} \tag{4.10}$$

The variables I_1, V_2, I_5, I_7, V_9 and I_{11} are given by the following relations :

$$K_p = R_L/(Z_2 + R_L).$$

$$I_{11} = (V_5 - V_{11} - V_7 - V_r K_p)/Z_2 K_p \tag{4.11}$$

$$I_7 = I_8(t) + I_9 + I_{11} \tag{4.12}$$

$$I_1 = (V_i - V_1 + I_2 R_4 - V_5)/(Z_1 + R_4) \tag{4.13}$$

$$V_2 = V_i - Z_1 I_1 - V_1 - V_3 \tag{4.14}$$

$$V_9 = V_{11} + V_r K_p + Z_2 I_{11} K_p - V_{10} \tag{4.15}$$

$$I_5 = I_1 - I_2 - I_7 - V_5/R_6 \tag{4.16}$$

Initialization of state variables is done by d.c. analysis of the equivalent circuit given in Fig. 4.1. The relations can be given as follows.

$$V_5 = V_3 R_6/(R_6 + R_4)$$

$$V_1 = -V_3$$

$$I_2 = -V_3/(R_6 + R_4)$$

$$V_7 = V_5 - V_{10}$$

$$I_9 = -I_D$$

$$V_{11} = -V_{10}$$

The computational procedure for the transient analysis of the circuit may be summarized as follows. At t = 0, values of the state variables are calculated from the d.c. analysis. At time instant t these are known from the previous history of the circuit, i.e., from the value of the state variable,

at the instant $(t - \Delta t)$ and its derivative value at that instant. $V_i(t)$ and $V_r(t)$ are obtained from transient analysis of the input and output transmission lines and are used for calculating the various state variable derivatives by equations 4.5 to 4.16. Similarly, values of the state variables at the time instant $(t + \Delta t)$ are evaluated by the use of state variables and its derivatives calculating at the time instant t and so on. Values of $V_{in}(t)$, $I_{in}(t)$, $V_{out}(t)$ and $I_{out}(t)$ which are required for continuing the transient analysis of the input and output transmission lines are obtained by use of equations 4.1 to 4.4. In order to incorporate the intrinsic transistor delay τ in the analysis, it is necessary to store the value of the drain current I_g over a time interval $(t - \tau)$ to t. Computer program developed for analysis of common source amplifier using the above procedure is given in Appendix I.

4.2 Results

The detailed circuit configuration used for this analysis has been given in figure 1.2 of chapter 1. It consists of a suitably biased MESFET in common source configuration. An uniform transmission line section of length L is connected at the input and the output is terminated by a load resistance R_L. Input pulse is applied at the far end of the transmission line section connected at input. A source resistance R_s whose value is equal to the characteristic impedance Z_o is connected in series with an ideal voltage pulse generator to ensure that

there is no multiple reflections in the transmission line. The length of the transmission line ensures that the input pulse dies away before the reflections from MESFET reach back to the source.

The MESFET D.C. characteristics used correspond to the measured D.C. characteristics of plessey GAT3 field effect transistor in microstrip package. For other elements of the MESFET equivalent circuits, typical guessed values have been used and may not correspond to the specified values of GAT3. Referring to Fig. 4.1. various values used in the computer simulation are

$C_1 = C_{11} = 120$ pf

$L_2 = L_9 = 0.5$ nH

$R_4 = 10$ ohms

$C_o = 0.4$ pF

$V_b = 0.1$ volt

$I_s = 1$ nA

$T = 300^oK$

$C_7 = 0.02$ pF

$I_{sat} = 28$ mA

$\tau = 5$ psec

$V_p = 5.1$ volt

$V_{10} = 5$ volt

Values of V_b, I_{sat}, V_p, A and B are evaluated from the measured characteristics given by the mathematical relations (2.4) and (2.5). Others are typical values as used for operation of MESFET at microwave frequency.

Computer simulation has been carried out to study effects of the variations in the following parameters,

i) Gate bias

ii) Characteristic impedance

iii) Gate series resistance R_4, and

iv) The intrinsic delay in the transistor τ.

The results are summarised in the following paragraph. For all these simulations, triangular pulses with rise and fall time of 10 pico-second and peak amplitude 5 volts have been considered. Both the positive and negative going pulses have been studied. The results shown in Fig. 4.2 to Fig. 4.9, depict the incident and reflected voltage waveforms at the FET input (at the terminals AA in Fig. 1.2) and the output voltage waveform across the load resistance R_L.

The following definitions of delay time and rise time are used for interpretation of the result.

Delay Time : It is the time measured between half the peak amplitude points of the incident pulse and the pulse to be measured.

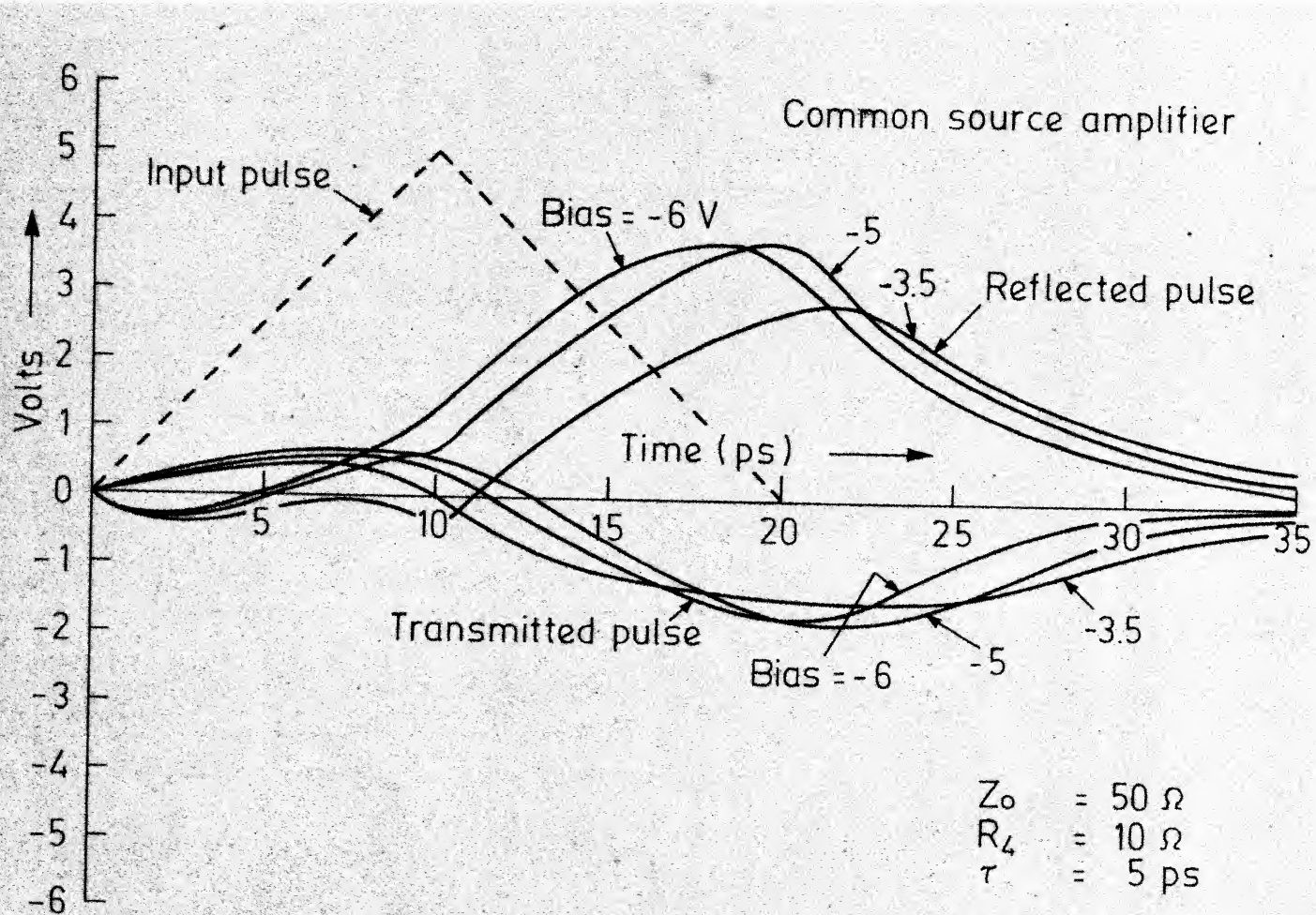


Fig. 4.2 - Effect of gate bias variation on a positive going pulse.

Rise Time : It is defined by the time to reach from 10 percent to 90 percent of the peak level.

(i) Effect of Gate bias variation

Positive Going Pulse :

The effect of variations in the gate bias for a positive going pulse is shown in Fig. 4.2. Bias levels selected are -6.0 V (beyond cut-off), -5.0 V(equal to cut-off) and -3.5 volt (before cut-off). For transmitted pulses the delays in the three cases are 11.2, 10.1 and 7.8 respectively.

Table 4.1

Effect of bias level on a positive going pulse

Bias (volts)	Delay (Ps)	Amplitude (volts)	Rise time (Ps)
Transmitted Pulse :			
-6	11.2	1.8	6.0
-5	10.1	1.8	6.6
-3.5	7.8	1.45	5.8
Reflected Pulse :			
-6	6.4	3.7	8.4
-5	7.9	3.8	9.4
-3.5	10.3	2.75	6.9

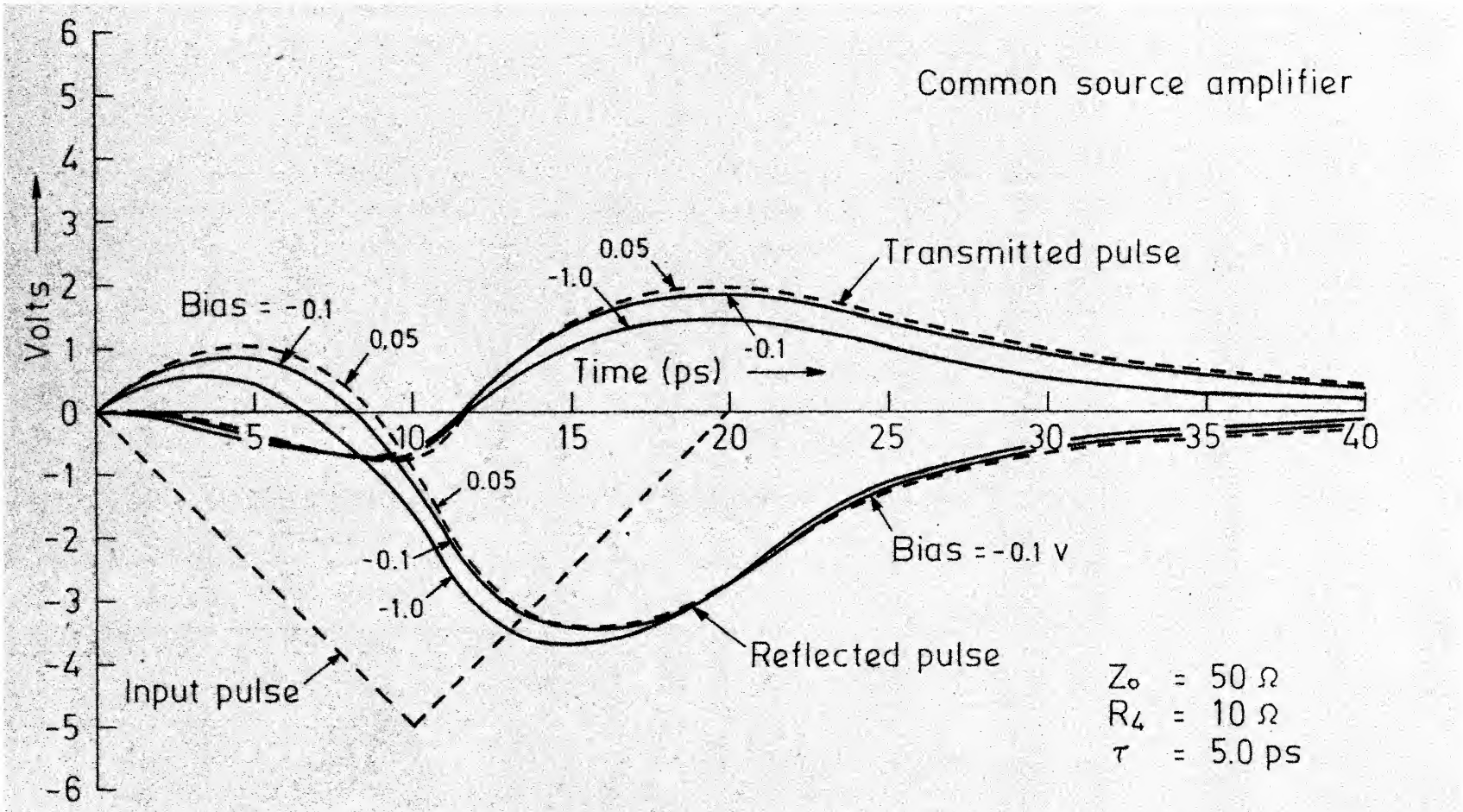


Fig. 4.3 - Effect of gate bias variation on a negative going pulse.

The intrinsic transistor of 5 ps. delay is included in the transmitted pulse delay. The remaining 6.2, 5.1 and 2.8 ps are perhaps, to a large extent, accounted by the charging time of the gate capacitance. When the bias is -3.5 V, the transmitted pulse is flattened, because of the input diode clamping. Results for rise time and delay time of the transmitted and reflected pulses at different bias points are summarized in Table 4.1. All the three rise times of the transmitted pulses are shorter than the corresponding rise time (8 ps) of the incident pulse.

Reflection delay varies considerably with bias and increases for less negative bias level. This is perhaps because of increased input capacitance. Amplitude of the reflected pulse is lower for bias at -3.5 V, again because of clamping by the input diode. The minimum rise time for reflected pulse is at the bias -3.5 V.

Negative Going Pulse

Effect of bias variation on a negative going triangular pulse is shown in Fig. 4.3. Three bias levels -1.0, -0.1 and +0.05 volts are considered. The main features of these results are given in Table 4.2.

For transmitted pulse the peak amplitude of the output pulse increases with the bias level. This is because of the increase in transconductance of MESFET. For the reflected pulse on the otherhand, the amplitude is higher for lower bias (-1.0 V). This is due to the smaller value of input

Table 4.2

Effect of bias level on a negative going pulse

Bias (volts)	Delay (ps)	Amplitude (V)	Rise Time (ps)
Transmitted Pulse :			
-1.0	8.7	1.45	5.5
-0.1	8.6	1.85	5.0
+0.05	8.8	2.0	4.9
Reflected Pulse :			
-1.0	5.3	3.7	5.1
-0.1	5.8	3.45	4.2
+0.05	5.9	3.4	4.1

capacitance for these bias levels.

Delay and the rise times for all the bias levels are smaller than the corresponding values for the positive going pulse.

(ii) Effect of impedance of the input line :

Positive Going Pulse :

The effect of variation in the characteristic impedance of the transmission line connected at the input is shown in Fig. 4.4. The main observations from this figure is

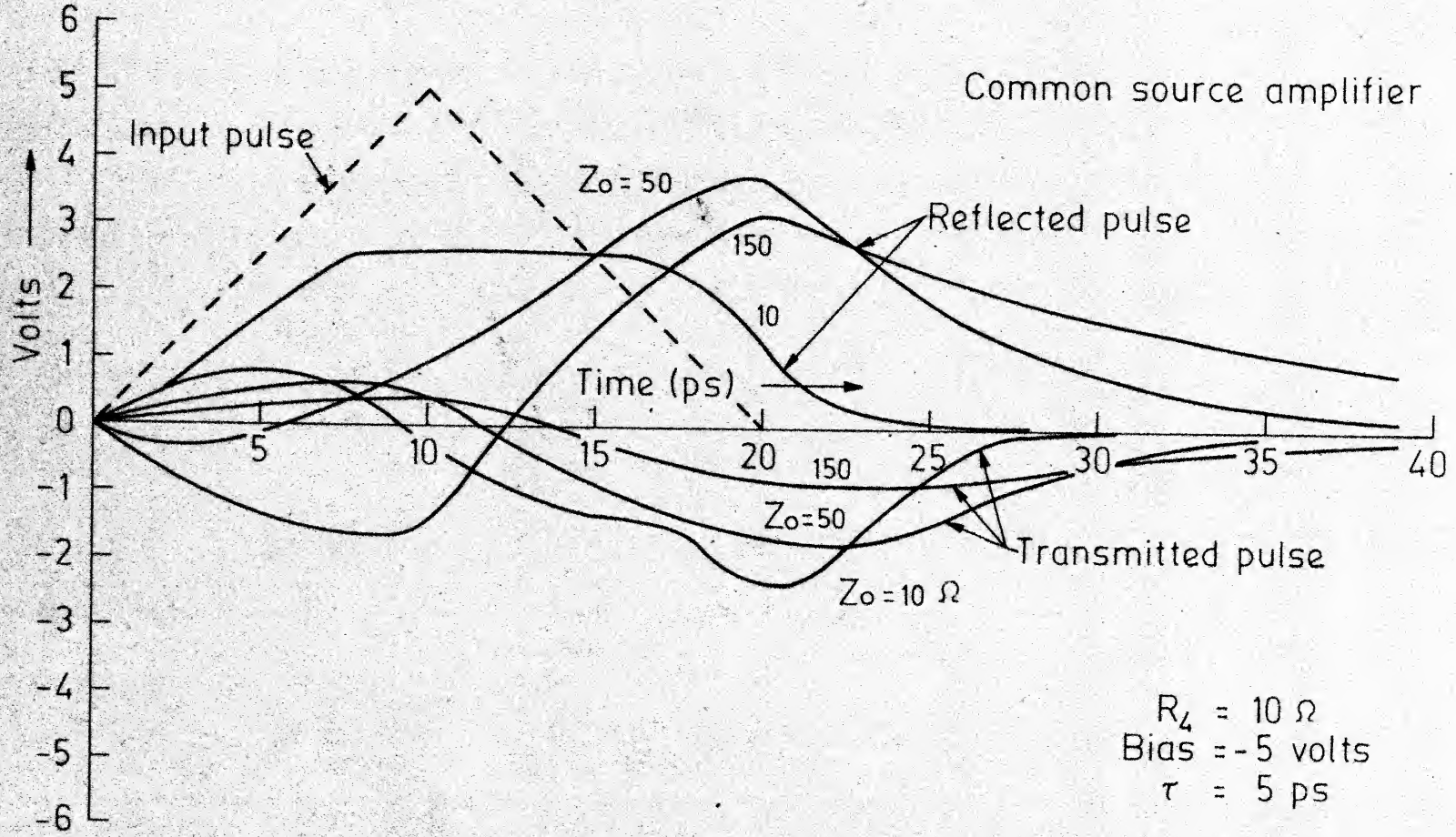


Fig. 4.4 - Effect of variations in the impedance of the input line on a positive going pulse.

Table 4.3

Effect of input line impedance on a positive going pulse

Impedance (ohms)	Amplitude (volts)	Delay (ps)	Rise time
Transmitted Pulse :			
10	2.4	8.4	9.4
50	1.8	10.2	7.4
150	0.9	12.0	5.8
Reflected Pulse :			
10	2.59	-0.9	5.6
50	3.8	8.0	11.0
150	3.25	10.5	5.8

summarised in Table 4.3.

This impedance value influences the delay time both for transmitted and reflected pulses. In general the delay increases with the impedance level. For the transmitted pulse, the pulse amplitude decreases when the input line impedance is increased. This is because of the fact that the charging time increases and the pulse cannot attain - its maximum value before the input pulse starts decaying. Another unusual feature is the clamping of the reflected pulse for low value of characteristic impedance of the

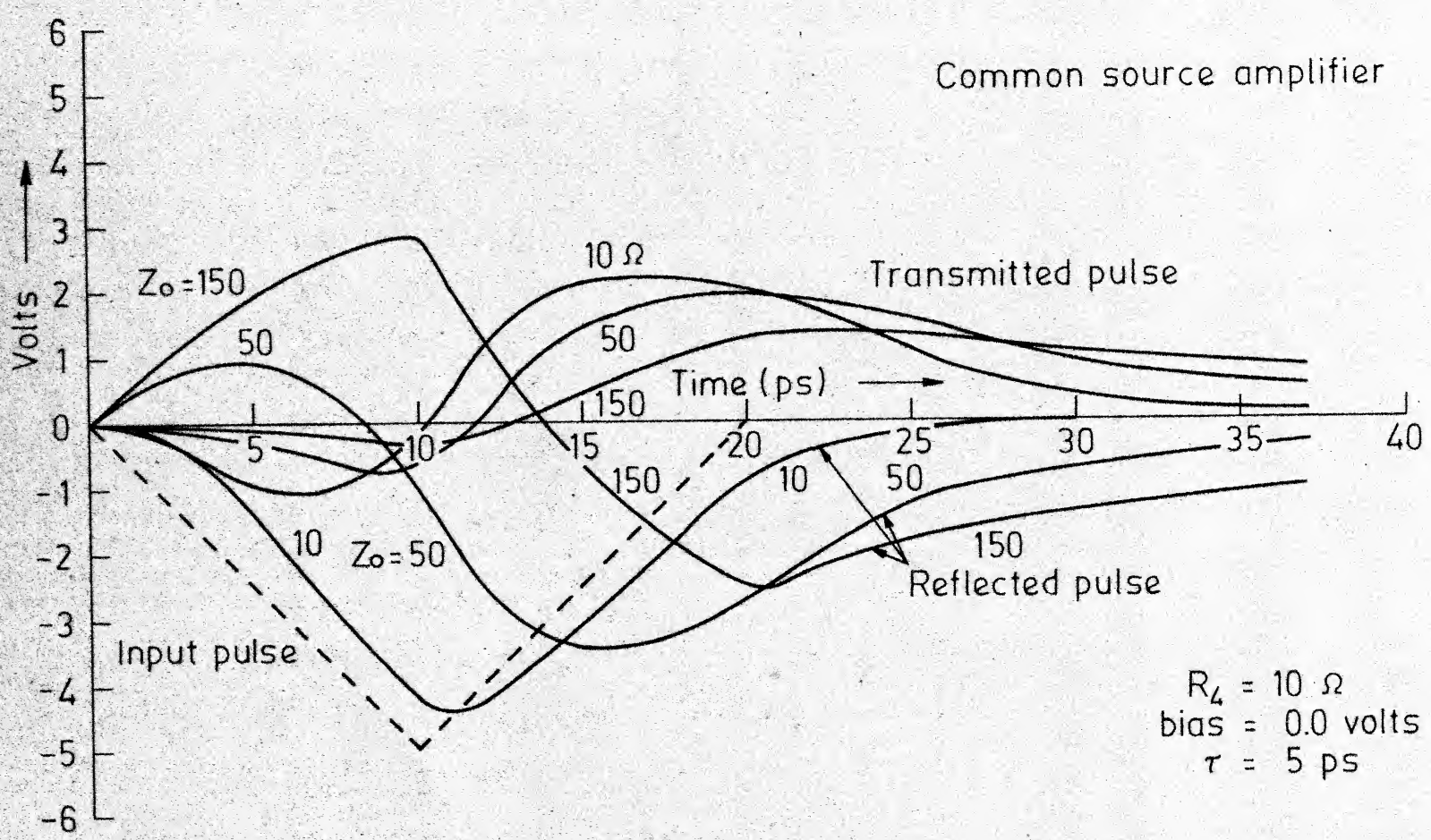


Fig. 4.5 - Effect of variation in the input line on a negative going pulse.

input line. It appears to be associated with the directly fed through portion of transmitted pulse. Another interesting feature is the initial negative portion of the reflected pulse for high impedance level of 150 ohms.

For the initial portion of the incident pulse, gate capacitance appears as a short circuit and is reponsible for negative reflection coefficient.

Negative Going Pulse :

Table 4.4

Effect of input line impedance on a negative going pulse

Impedance (ohms)	Amplitude (volts)	Delay (ps)	Rise time (ps)
Transmitted Pulse :			
10	2.2	6.8	3.4
50	1.95	8.7	5.1
150	1.3	10.9	5.8
Reflected Pulse :			
10	4.45	1.4	6.5
50	3.45	5.9	4.2
150	2.55	11.3	4.7

Effect of the impedance of the input line on a negative going pulse is shown in Fig. 4.5. The main features of these

results are tabulated in Table 4.4. Pulse delay times follow variation similar to those for positive going pulse. Again the minimum delay is obtained for lower impedance line. Clamping of the reflected pulse is not present now although there is considerable rounding of for 50 ohm impedance level.

From the results shown in the Figs. 4.4 and 4.5 it may be concluded that it is advantageous to use low impedance lines for MESFET pulse amplifier.

(iii) Effect of Gate Series Resistance :

Effect of variations in the value of series resistance of the gate junction is shown in Fig. 4.6 and 4.7 for positive and negative going pulses respectively. Tables 4.5 and 4.6 summarize the main observations obtained from figures 4.6 and 4.7. Value of gate series resistance depends on device parameters of MESFET and bonding used. The aim of this study is to find out whether the value of this resistance is critical for the operation of MESFET pulse amplifier.

The value of R_4 (gate series resistance) selected for circuit simulation are 10, 5 and 1 ohms. In all the cases the characteristic impedance Z_o of the input line is taken as 10 ohms because at low value of Z_o the value of R_4 becomes more significant. Results shown in Fig. 4.6 and 4.7 show that value of R_4 is not significant except when reflection for

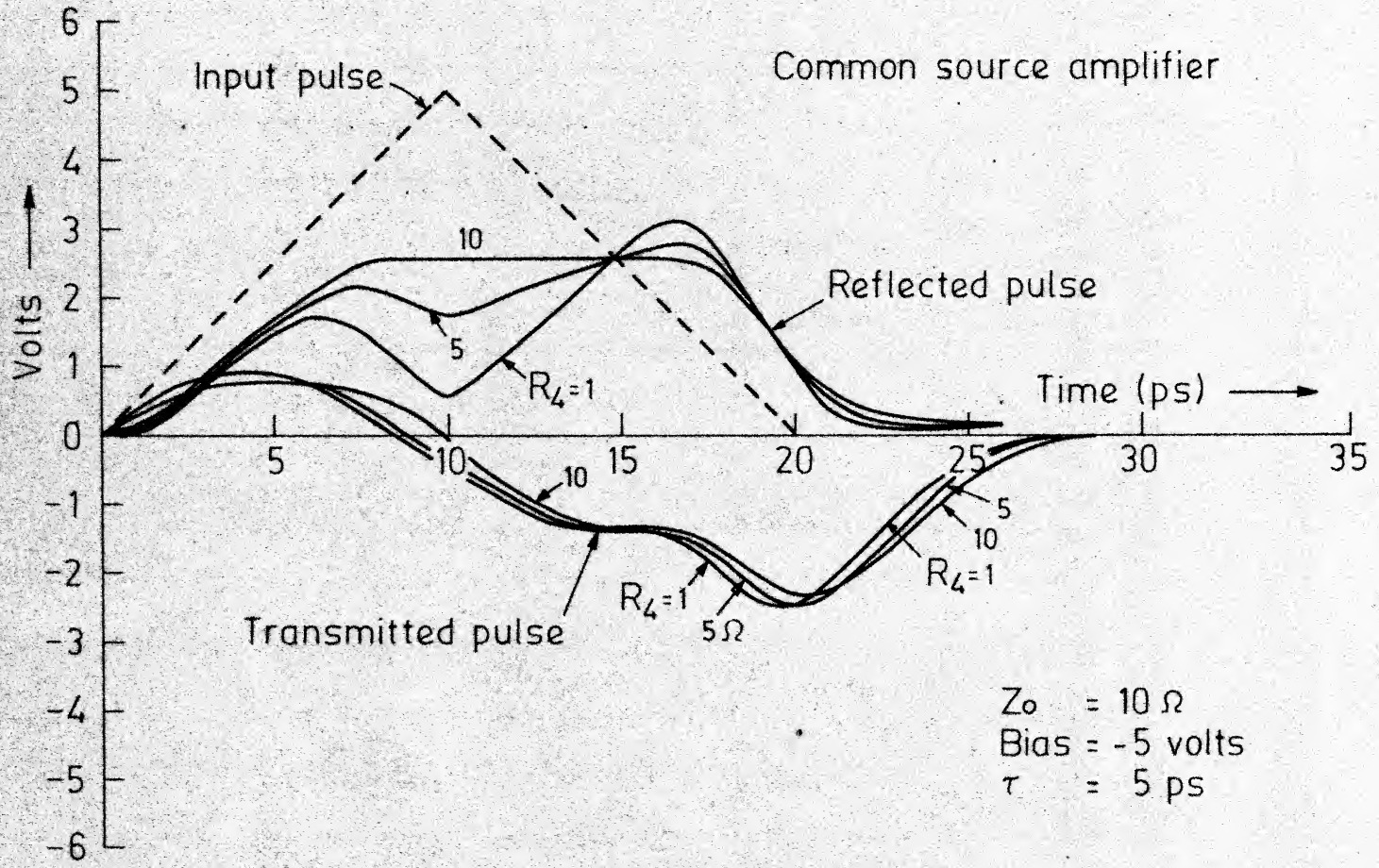


Fig. 4.6 - Effect of variations in the gate series resistance on a positive going pulse.

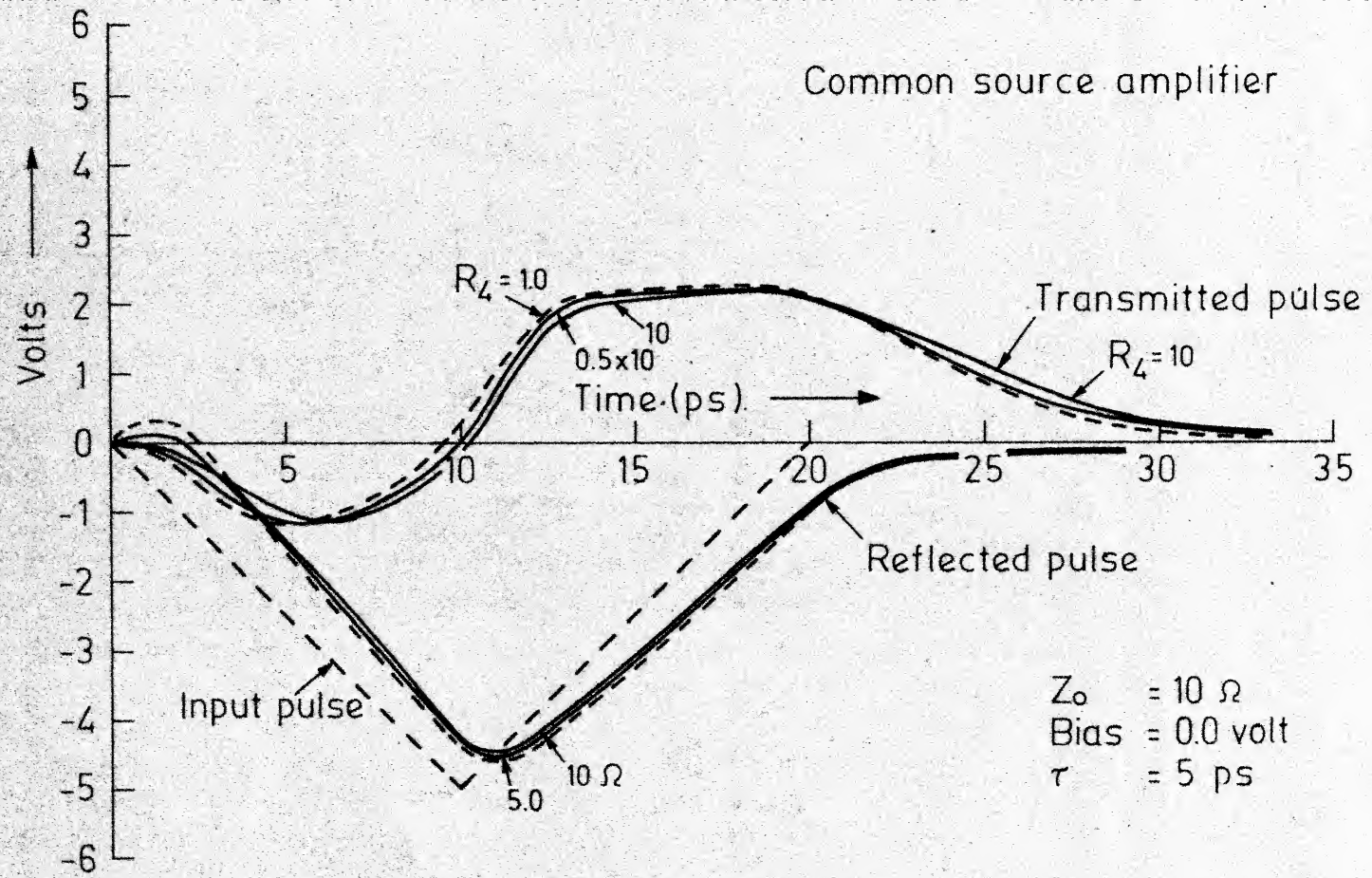


Fig. 4.7 - Effect of variation in gate series resistance on a negative going pulse.

positive going pulse is considered. The strange behaviour seen in this case is related to clamping of the input pulse for low value of Z_o, and is discussed in previous section.

Table 4.5

Effect of gate series resistance

R_4 (ohms)	Amplitude (volts)	Delay (ps)	Rise time (ps)
Transmitted Pulse :			
10	2.4	8.4	9.4
5	2.5	8	9.2
1	2.5	7.6	9.3
Reflected Pulse :			
10	2.59	-0.9	5.6
5	2.8	-0.4	12.9
1	3.1	0.4	13.3

Table 4.6

R_4 (ohms)	Amplitude (volts)	Delay (ps)	Rise time (ps)
Transmitted Pulse :			
10	2.15	6.6	3.2
5	2.2	6.4	2.8
1	2.3	6.3	3.2
Reflected Pulse :			
10	4.45	1.4	7.2
5	4.55	1.4	6.6
1	4.65	1.2	5.6

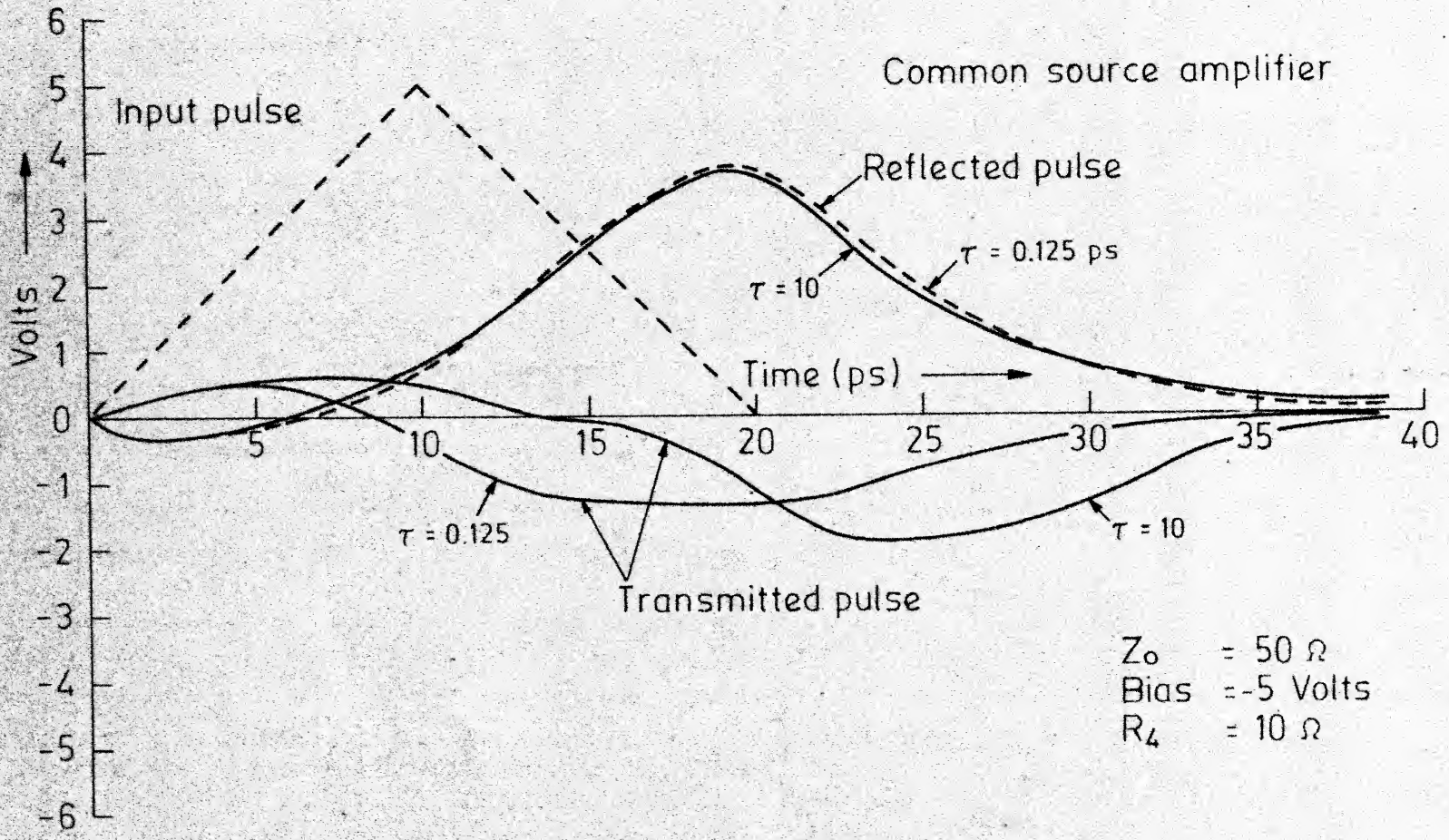


Fig. 4.8 - Effect of variations in intrinsic delay on a positive going pulse.

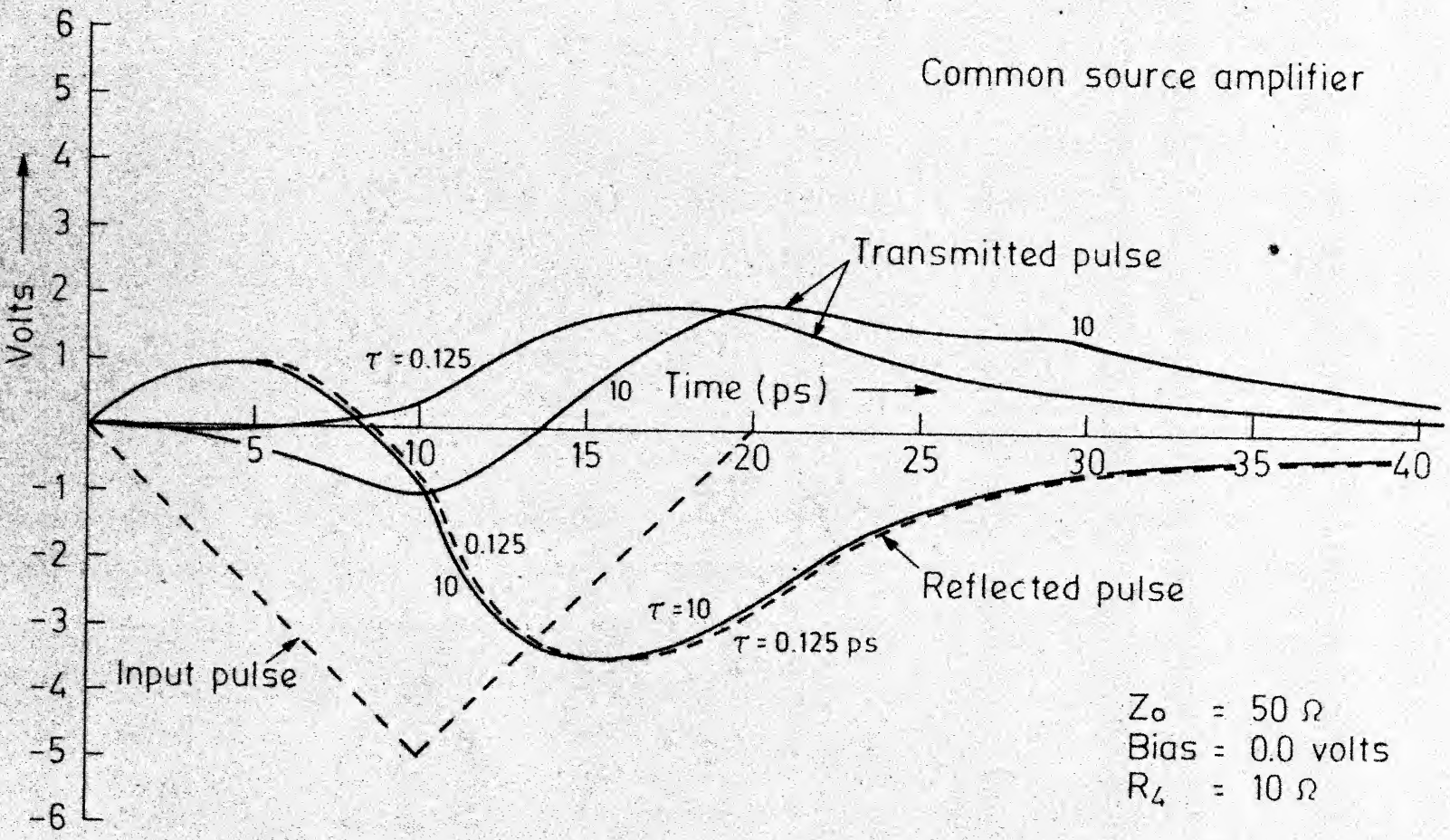


Fig. 4.9 - Effect of variation of intrinsic transistor delay on a negative going pulse.

(iv) Effect of Intrinsic Delay in MESFET

The effect of changes in the intrinsic delay in the MESFET is shown in Fig. 4.8 and 4.9 for positive going and negative going pulses respectively. Since it is difficult to find the accurate value of intrinsic delay in the transistor, it is desirable to know the effect of variations in this value. As seen from these figures, there is hardly any change in the reflected pulse when the intrinsic delay τ varies from 0.125 ps to 10 ps. Of course the delay in the transmitted pulse increases with the increase of intrinsic delay in the transistor. These results are summarized in Table 4.7.

Table 4.7
Effect of intrinsic transistor delay

Pulse Type	Intrinsic delay	Pulse delay
Transmitted pulse :		
Positive going	0.125	6
Positive going	10	14.4
Negative going	0.125	7.9
Negative going	10	11.2

Chapter 5

COMMON SOURCE PULSE AMPLIFIER CONFIGURATION WITH ACTIVE LOAD

5.1 Transient Analysis

The logic gate design that has been used for the fastest GaAs MESFET logic uses active loads.[14] Active loads help in providing a high output impedance at the output in monolithic GaAs digital ICs.

The circuit configuration considered for analysis and its equivalent circuit is shown in Fig. 5.1. For analysing the circuit we use the same procedure (analysis using state valuables) was used in analysing pulse amplifier without active load. Considering the voltage across capacitors and current across inductors as state variables, the input and output currents can be expressed in terms of state variables as

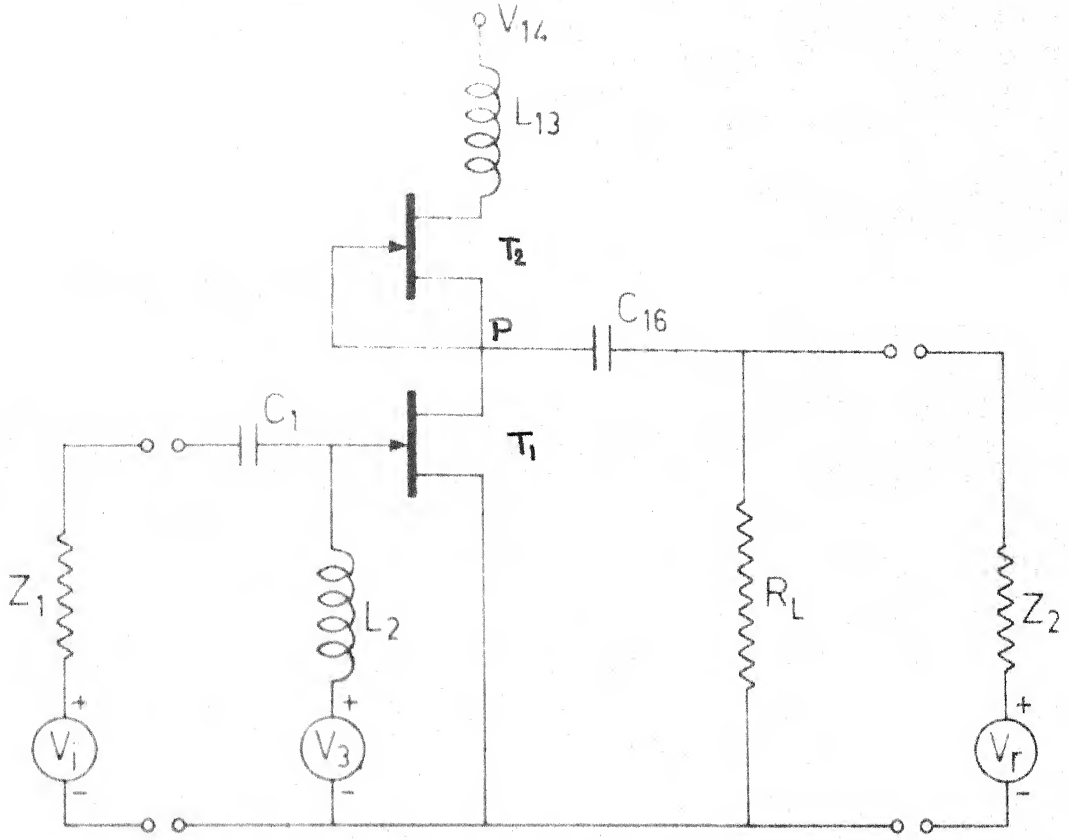
$$I_{in} = C_1 \frac{dV_1}{dt} \tag{5.1}$$

$$I_{out} = C_{16} \frac{dV_{16}}{dt} \left(\frac{R_1}{Z_2 + R_L}\right) - \frac{V_r}{R_L + Z_2} \tag{5.2}$$

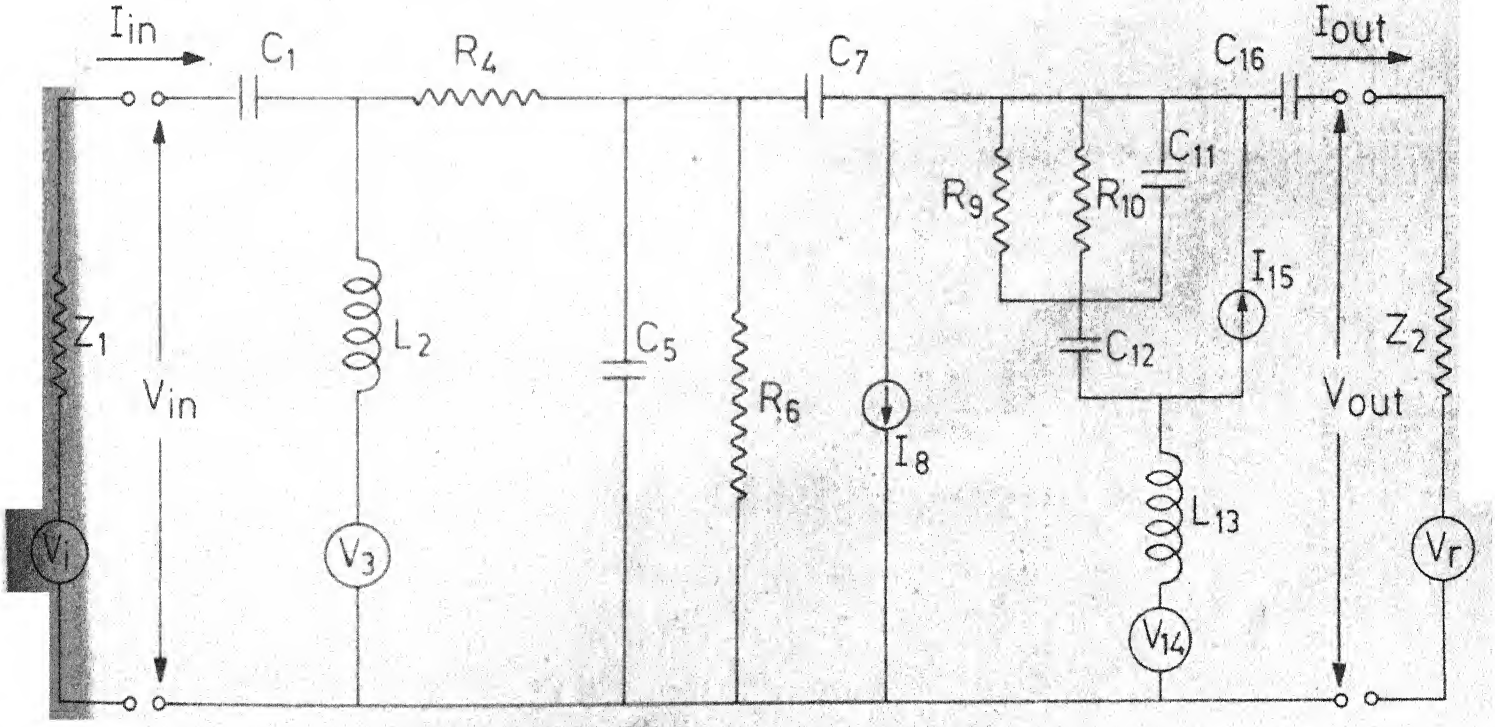
As before V_i and V_r, two parameters introduced for convinience of transmission line transient analysis, are defined as

$$V_i = V_{in} - Z_1 I_{in} \tag{5.3}$$

$$V_r = V_{out} - Z_2 I_{out} \tag{5.4}$$



(a)



(b)

Fig. 5.1 - MESFET in common source with active load configuration with biasing network and input - output transmission line equivalent circuit.

where Z_1 is the impedance of the input line and Z_2 is the impedance of the output line.

The sign convention used for analysis of this circuit remains the same as in previous circuit (See Sec. 4.1). R_L is a resistor connected across the output to limit the output voltage swings even when reflection from the transmission line connected at the output terminal are unfavourable. Its impedance value is so high (10 K ohms) that one can approximate it with an open circuit. Capacitors C_1 and C_{16} are used for blocking the d.c. voltages. For biasing, inductors are used. From equivalent circuit (Fig. 5.1) it is seen that battery V_{14} and current source I_{15} will connect directly if no inductor (L_{13}) is used in between. So an inductor having a very small value of inductance (0.5 pH) is connected in between the battery and the current source without much reducing the speed of the circuit.

Derivatives of the state variables used for finding I_{in}, I_{out} and updating the values of the state variables are derived by writing the circuit equations based on Kirchoff's law. These circuit equations may be written as

$$\frac{dV_1}{dt} = I_1/C_1 \qquad (5.5)$$

$$\frac{dI_2}{dt} = V_2/L_2 \qquad (5.6)$$

s $$\frac{dV_5}{dt} = I_5/C_5 \tag{5.7}$$

$$\frac{dV_7}{dt} = I_7/C_7 \tag{5.8}$$

$$\frac{dV_{11}}{dt} = I_{11}/C_{11} \tag{5.9}$$

$$\frac{dV_{12}}{dt} = I_{12}/C_{12} \tag{5.10}$$

$$\frac{dV_{13}}{dt} = V_{13}/L_{13} \tag{5.11}$$

$$\frac{dV_{16}}{dt} = I_{16}/C_{16} \tag{5.12}$$

The variables I_1, V_2, I_5, I_7, I_{11}, I_{12}, V_{13} and I_{16} can be found out from the following relations formed by using Kirchoff's law.

$$K_p = R_L/(R_L + Z_2)$$

$$I_{16} = (V_5 - V_{16} - V_7 - V_o K_p)/Z_2 K_p \tag{5.13}$$

$$V_{13} = V_5 - V_{12} - V_{14} - V_7 - V_{11} \tag{5.14}$$

$$I_{12} = I_{13} + I_{15}(t) \tag{5.15}$$

$$I_{11} = I_{12} - V_{11}/R_K \tag{5.16}$$

$$I_7 = I_8(t) + V_{11}/R_K + I_{16} + I_{11} - I_{15}(t) \tag{5.17}$$

$$I_1 = (V_I - I_2 R_4 - V_1 - V_5)/(Z_1 + R_4) \tag{5.18}$$

$$V_2 = V_I - (Z_1 I_1 + V_1 + V_3) \qquad (5.19)$$

$$I_5 = I_1 - I_2 - I_7 - V_5/R_6 \qquad (5.20)$$

where $R_K = R_9 \parallel R_{10} = R_9 R_{10}/(R_9 + R_{10})$

D.C. analysis of the circuit required for initialisation of state variables is done as follows. The d.c. condition of the circuit (i.e. all the current and voltages in the circuit equivalent circuit) is known if the voltage at the point P Fig. (5.1.a) can be calculated for a particular set of battery voltages in the circuit. For solving this numerically the condition utilised is that at the point P, $I_{D1} = I_{D2}$ where I_{D1} is the drain current in T_1 and I_{D2} is the drain current in T_2. First it is assumed that both the transistors are in saturation condition and the drain currents through the transistors are calculated for their respective gate biasing. If I_{D1} is greater than I_{D2} the actual current through the point P is given by $I_D = I_{D2}$ and the transistor T_1 is not in saturation. If the voltage at the point P is X, I_D can be written as :

$$I_D = A_1(X - B_1((X - V_5 + V_B)^{1.5} - (V_B - V_5)^{1.5})) \qquad (5.21)$$

where A_1 and B_1 are known quantities and depend on characteristics of a particular MESFET as discussed. The root of the equation (5.21) (which lies between X = 0 and X = $V_{\text{pinch off}} + V_{\text{gate bias}} - V_B$) is the value of the potential at the point P.

Again if I_{D1} is less than I_{D2}, we have $I_D = I_{D1}$ and T_2 is not in saturation. In this case the equation can be written as

$$I_D = A_2(V_{14} - X - B_2((V_{14} - X + V_B)^{1.5} - (V_B)^{1.5})) \qquad (5.22)$$

where V_B is the contact potential formed at the gate junction.

The root of this equation (which lies between $X = V_{14} - V_{pinch\ off} + V_B$ and $X = V_{14}$) is the solution for voltage at the point P which satisfies the above condition.

If $I_{D1} = I_{D2}$ it is justified to assume that the voltage at the point P is $V_{14}/2$.

So after solving this the d.c. condition or the initial value of the state variables can be written as :

$$I_{D15} = I_{D8}$$

$$V_{16} = X$$

$$V_{11} = 0$$

$$V_{12} = X - V_{14}$$

$$V_7 = V_5 - V_{16}$$

$$I_2 = -V_3/(R_4 + R_6)$$

$$I_{13} = -I_{D15}$$

$$V_1 = -V_3.$$

The detailed program developed for analysis of this circuit is attached in the Appendix III.

5.2 Results

The circuit configuration analysed is shown in Fig. 5.1. The only change as compared with the circuit shown in Fig. 4.1 is the load circuit. The purpose of this simulation is to study transmission and reflection of narrow pulses through a MESFET amplifier with the circuit configuration as shown in Fig. 5.1.

The MESFET characteristics used for amplifier correspond to the measured d.c. characteristics of a plessey GAT3 field effect transistor in a microstrip package. For all other elements of MESFET circuits, typical guessed values have been used. Referring to Fig. 5.1, various values used in computer simulation are

$C_1 = C_{16} = 120$ pF

$L_2 = 0.5$ nH

$L_{13} = 0.5$ pH

$R_9 = R_4 = 10$ ohms

$C_o = 0.4$ pF

$V_b = 0.1$ V

$I_s = 1$ nA

$T = 300^oK$

$C_7 = C_{12} = 0.02$ pF

For MESFET - T_1

I_{sat} = 28 mA

A = 16.14×10^{-3}

B = 0.2924

For MESFET - T_2

I_{sat} = 22 mA

A = 12.65×10^{-3}

B = 0.2924

τ = 5 psec.

V_p = 5.1 V

V_{14} = 10 V

Computer simulation has been carried out to study effects of variations of the following parameters on transmitted and reflected pulses.

i) Gate bias

ii) Characteristic impedance of the input line

iii) Gate series resistance R_4, and

iv) Intrinsic delay in the transistor τ

The main results of this analysis and comparison of the results with those for the previous circuit are summarized in the following paragraphs.

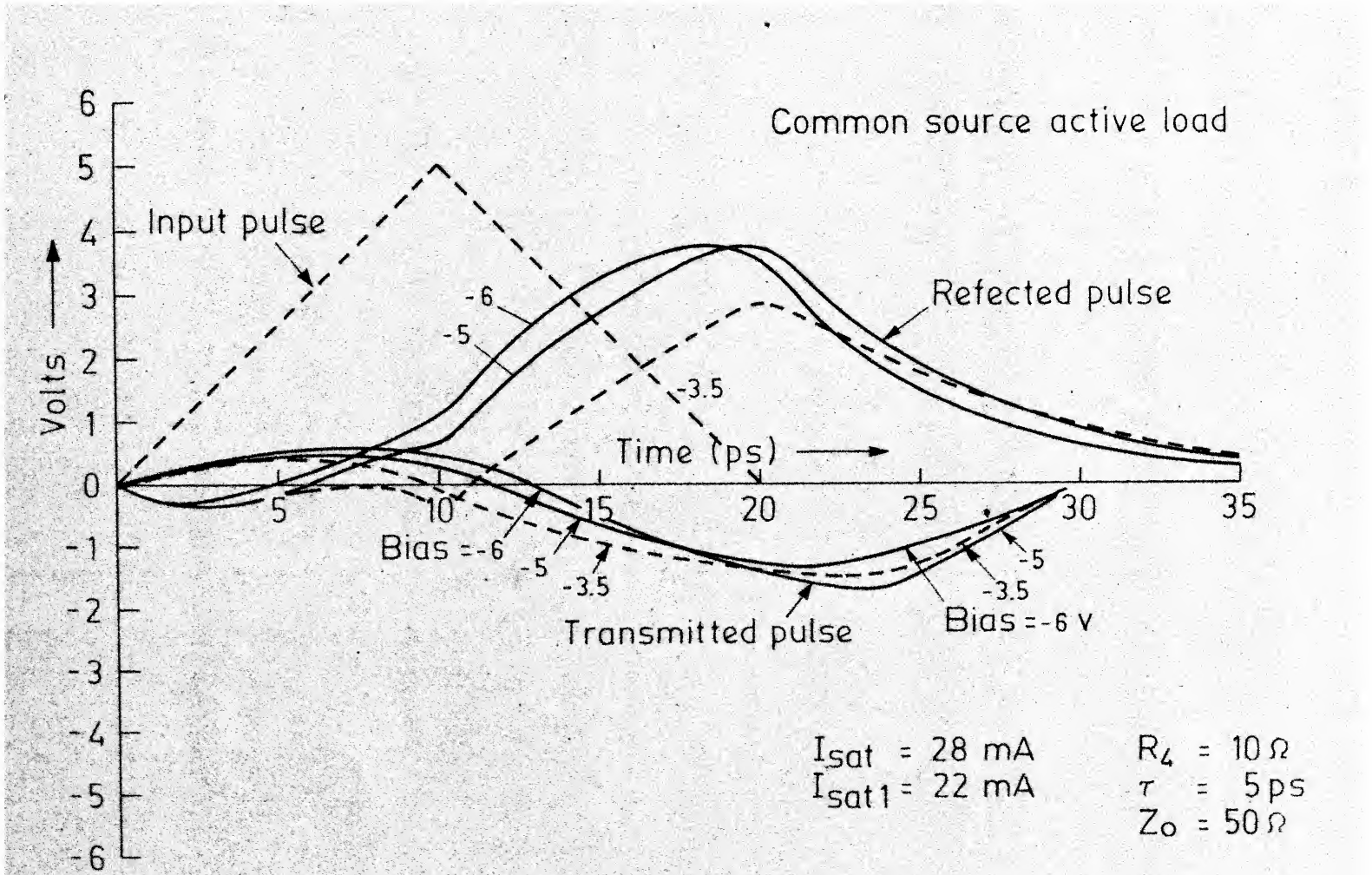


Fig. 5.2 - Effect of gate bias variation on a positive going pulse.

(i) Effect of Gate Bias Variation

Positive Going Pulse : The effect of variations in the gate bias for a positive going pulse is shown in Fig. 5.2. Bias levels selected are - 6.0 V (beyond cutoff), -5.0 V (equal to cutoff) and -3.5 V (above cutoff). Results for rise time and delay of the transmitted and reflected pulses at different bias points are summarized in Table 5.1. It is to be noticed, that the amplitudes, rise times and delays are almost of the same order as obtained in the previous circuit in Chapter 4. But it is clear that there is a sharp reduction in fall time in transmitted pulse for the active load circuit.

There is a small increase in rise time and delay of the transmitted pulse in the active load circuit. This is because when the amplifier transistor is in cut-off bias the load transistor behaves as short circuit with zero current. As the transmitted pulse amplitude depends on the output load impedance, the output pulse amplitude cannot attain high value so long the active load impedance is low and thereby the rise time increases. But this nonlinearity in output load helps discharging capacitors and reduces the fall time.

Comparing the equivalent circuits shown in Fig. 5.1 and 4.1, the input circuit remains practically the same for both the circuits, because the feedback capacitor C_7 is of very low value in both the cases. So the reflected

pulses are identical in the two circuits.

Table 5.1
Effect of bias level on a positive going pulse

Bias (volts)	Delay (ps)	Amplitude (volts)	Rise time (ps)
Transmitted Pulse :			
-6	11.2	1.35	6.5
-5	11.8	1.72	9.1
-3.5	8.8	1.52	10.0
Reflected Pulse :			
-6	6.4	3.7	6.4
-5	7.9	3.8	9.4
-3.5	10.3	2.75	6.9

Negative Going Pulse :

Effect of bias variation on a negative going triangular input pulse is shown in Fig. 5.3. Results are calculated for -1.0 V, -0.1 V and 0 volts. As the variation in output is not much only two sets of plots are shown in Fig. 5.3.

The main features of these results are given in Table 5.2. For the transmitted pulse, the peak value of amplitude of the output pulse increases with bias level, because of the

increase in transconductance. For the reflected pulse the amplitude is higher for lower bias as the input capacitance is low at this bias level.

Though the delay time for the transmitted pulses is increased, the fall time of the transmitted pulses is reduced considerably in active load circuit. The reason for this behaviour is same as given for positive going pulse.

Table 5.2

Effect of bias level on a negative going pulse

Bias (volts)	Delay (ps)	Amplitude (volts)	Rise time (ps)
Transmitted Pulse			
-1	8.6	1.25	8.4
0	9	1.5	11.6
Reflected Pulse			
0	5.6	3.45	4.2
-1	5.3	3.7	5.1

(ii) Effect of Variation in the Impedance of the Input Line

Positive Going Pulse

The effect of variation in characteristic impedance of the transmission line connected at the input is shown in

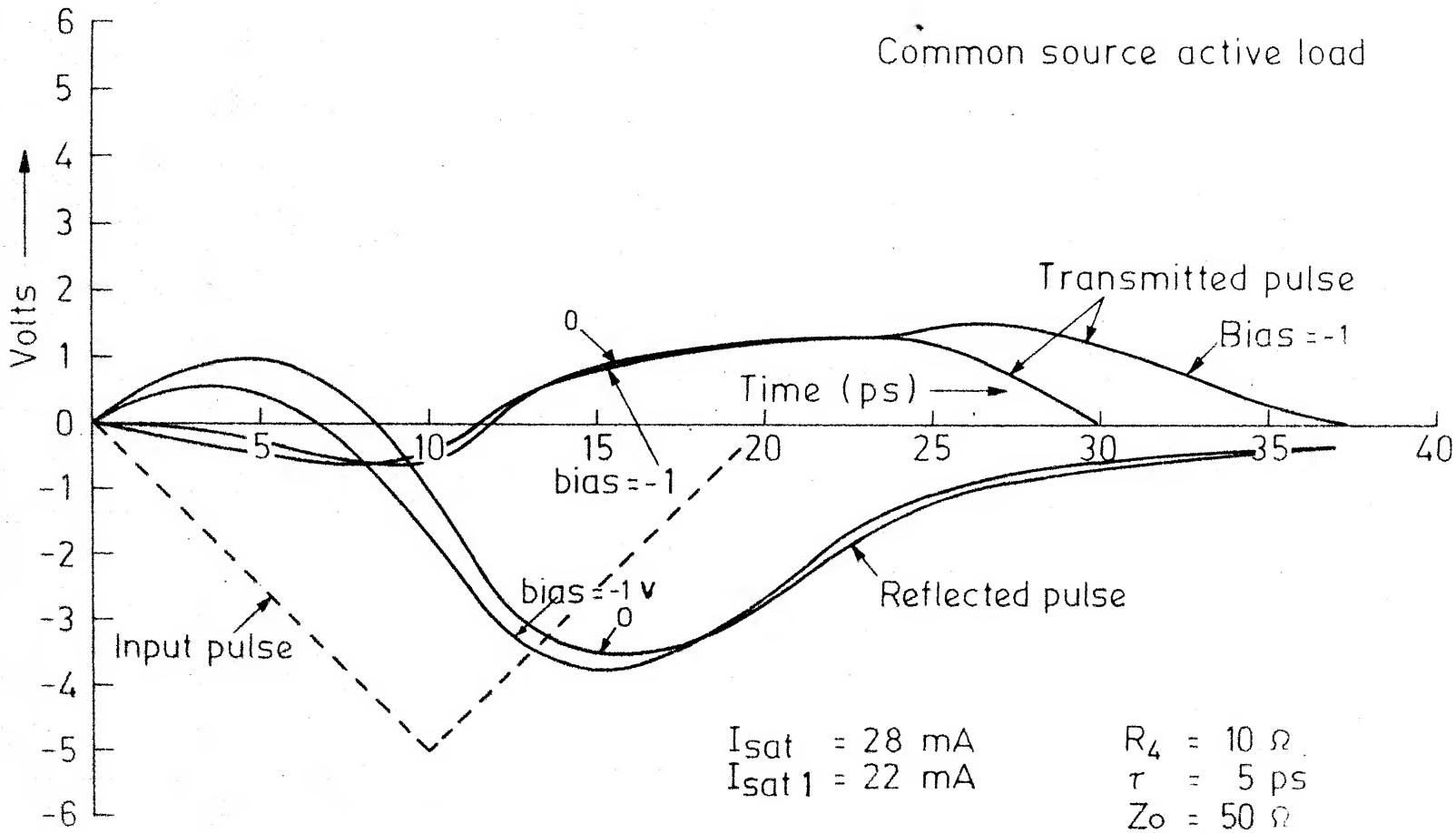


Fig. 5.3 - Effect of variation in gate bias on a negative going pulse.

Fig. 5.4. The main observations from the figure are summarized in Table 5.3.

For the transmitted pulse the amplitude decreases with increase of input line impedance. This is perhaps due to the charging time of the input capacitance which increases with increase in line impedance and can not attain the maximum value before the input starts decreasing.

Results for the reflected pulse remain the same as reported in Table 4.3. The unusual feature here is that the delay and the rise time in the transmitted pulse remain almost same with change in input line impedance. The nonlinearity of load impedance is responsible for this.

Table 5.3

Effect of input line impedance on a positive going pulse

Impedance (ohms)	Delay (ps)	Amplitudes (volts)	Rise time (ps)
Transmitted Pulse			
10	12.5	2.3	9.5
50	12	1.7	9.4
Reflected Pulse			
10	-0.9	2.59	5.6
50	8.0	3.8	11.0

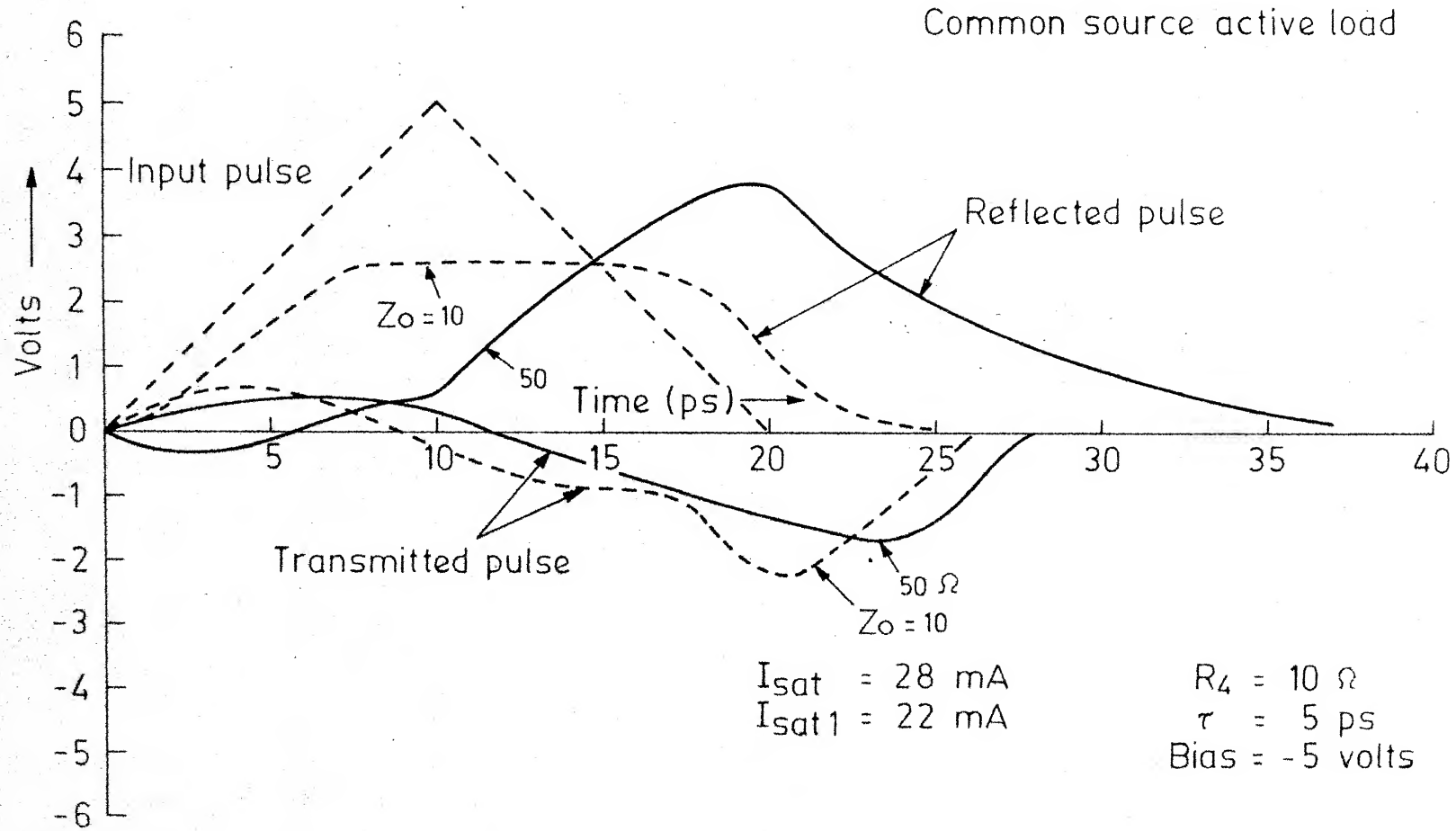


Fig. 5.4 - Effect of variation in input line on a positive going pulse.

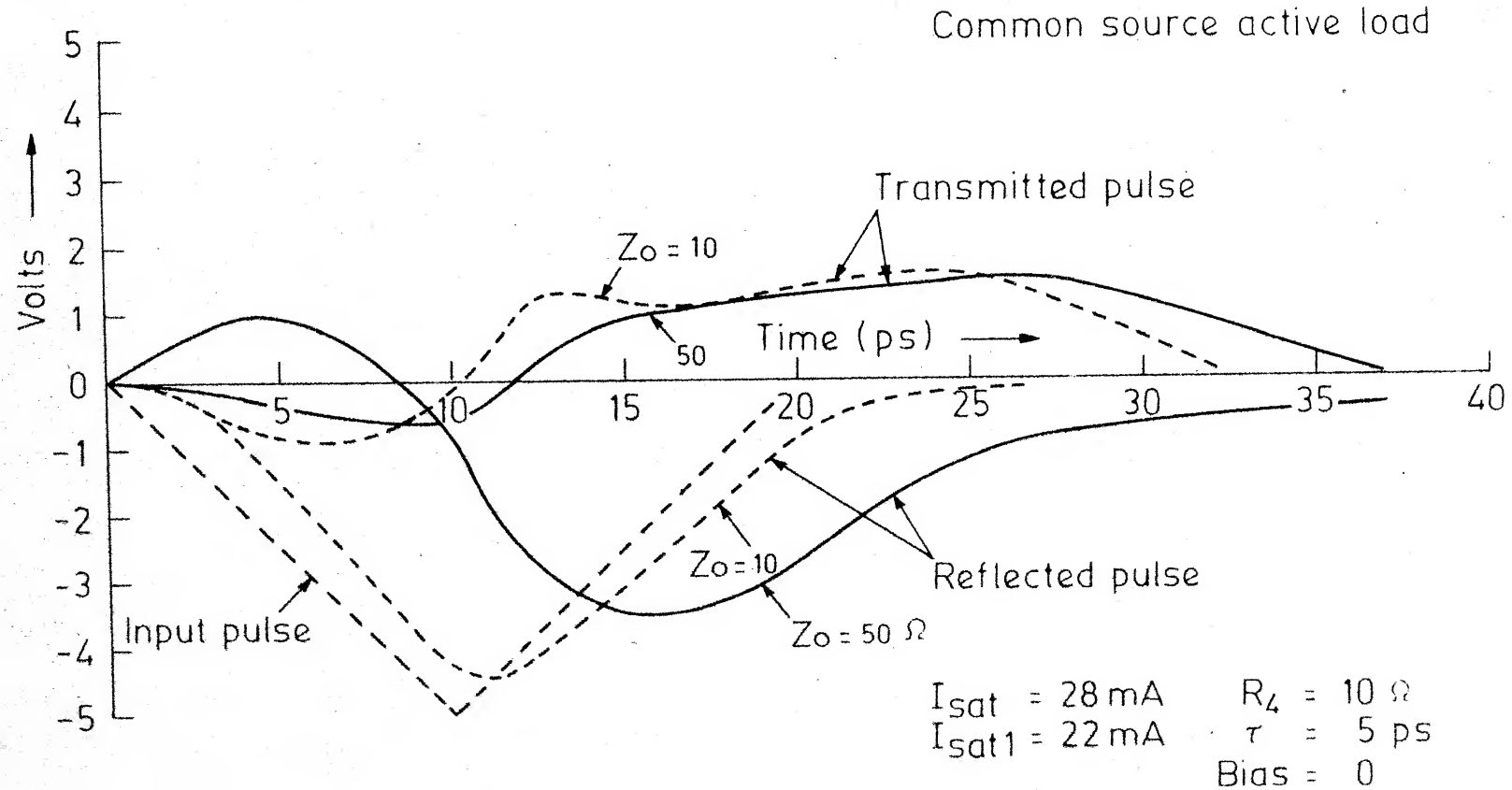


Fig. 5.5 - Effect of variation in input line impedance on a negative going pulse

Negative Going Pulse

Effect of the impedance of the input line on a negative going pulse is shown in Fig. 5.5. The main features of these results are tabulated in Table 5.4.

The pulse amplitude follows the same variation similar to those for positive going pulse. But in this case the delay increases with the impedance level. Though there is a considerable rounding effect the present case has no clamping effect in the reflected pulse.

From these results it may be concluded that the low impedance line is advantageous for the common source active load amplifier also.

Table 5.4

Effect of input line impedance on a negative going pulse

Impedance (ohms)	Delay (ps)	Amplitude (volts)	Rise time (ps)
Transmitted Pulse			
10	5.6	1.6	9.4
50	9	1.5	11.6
Reflected Pulse			
10	4.45	1.4	6.5
50	3.45	5.9	4.2

(iii) Effect of Gate Series Resistance

Effect of variation in the value of series resistance in the gate junction is shown in Fig. 5.6 and 5.7 for positive and negative going pulse respectively. The aim of this study is to find out a critical value of gate series resistance. Z_o is taken 50 ohms for positive going pulse and 10 ohms for negative going pulse. But from the Fig. 5.6 and 5.7 it is evident that the change in the value of R_4 does not have any significant effect on transmitted pulse. For reflected pulse the effect of R_4 is significant for a low input impedance line and this has been discussed earlier in Chapter 4. Table 5.5 and 5.6 summarized the main observations obtained from Fig. 5.6 and 5.7 respectively.

Table 5.5

Effect of gate series resistance on a positive going pulse

R_4 (ohms)	Delay (ps)	Amplitude (volts)	Rise time (ps)
Transmitted Pulse			
10	12	1.7	9.4
1	11.8	1.8	9.2
Reflected Pulse			
10	8.0	3.8	11.0
1	8.9	4.2	7.6

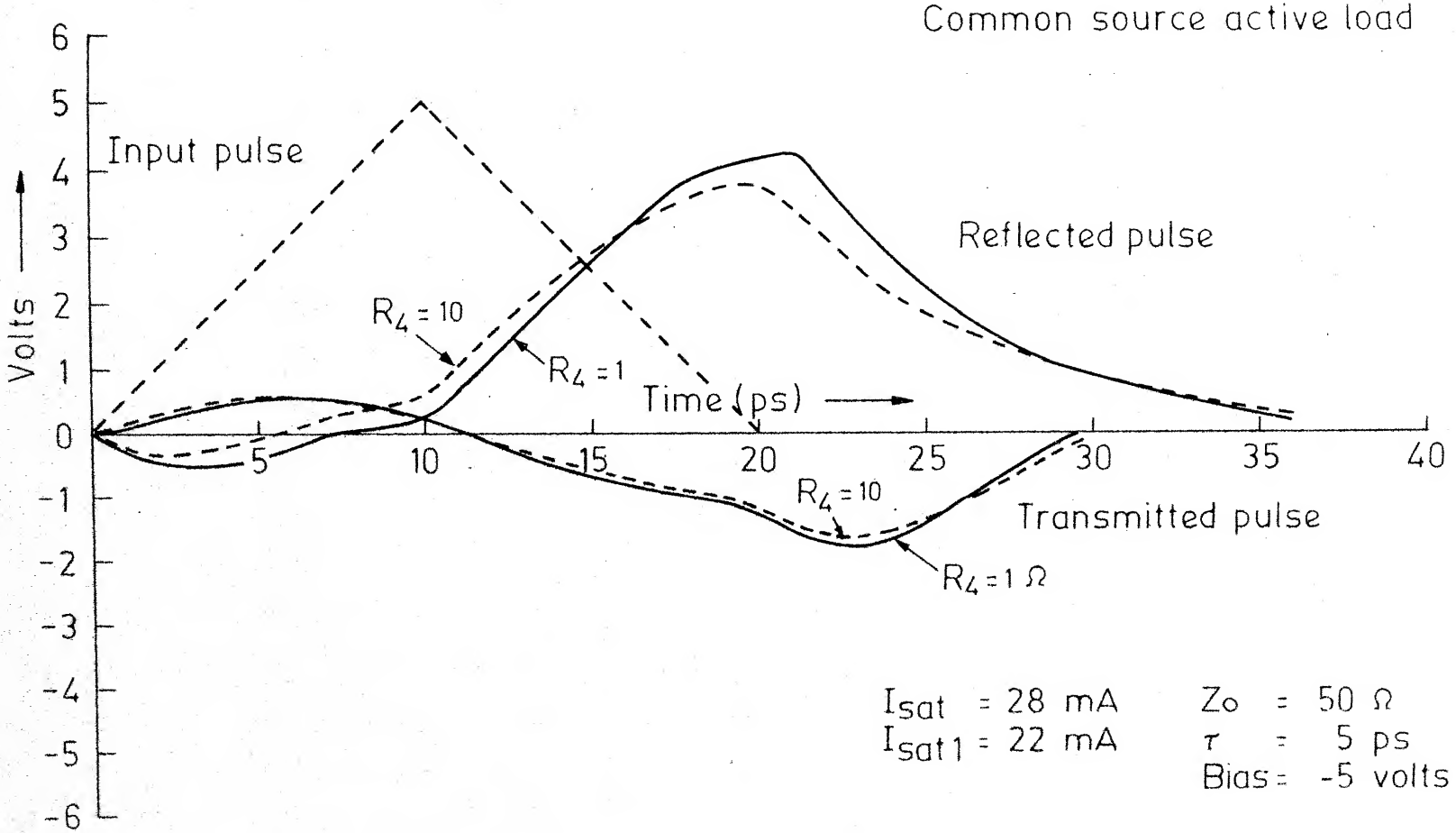


Fig. 5.6 - Effect of variation in the gate series resistance on a positive going pulse.

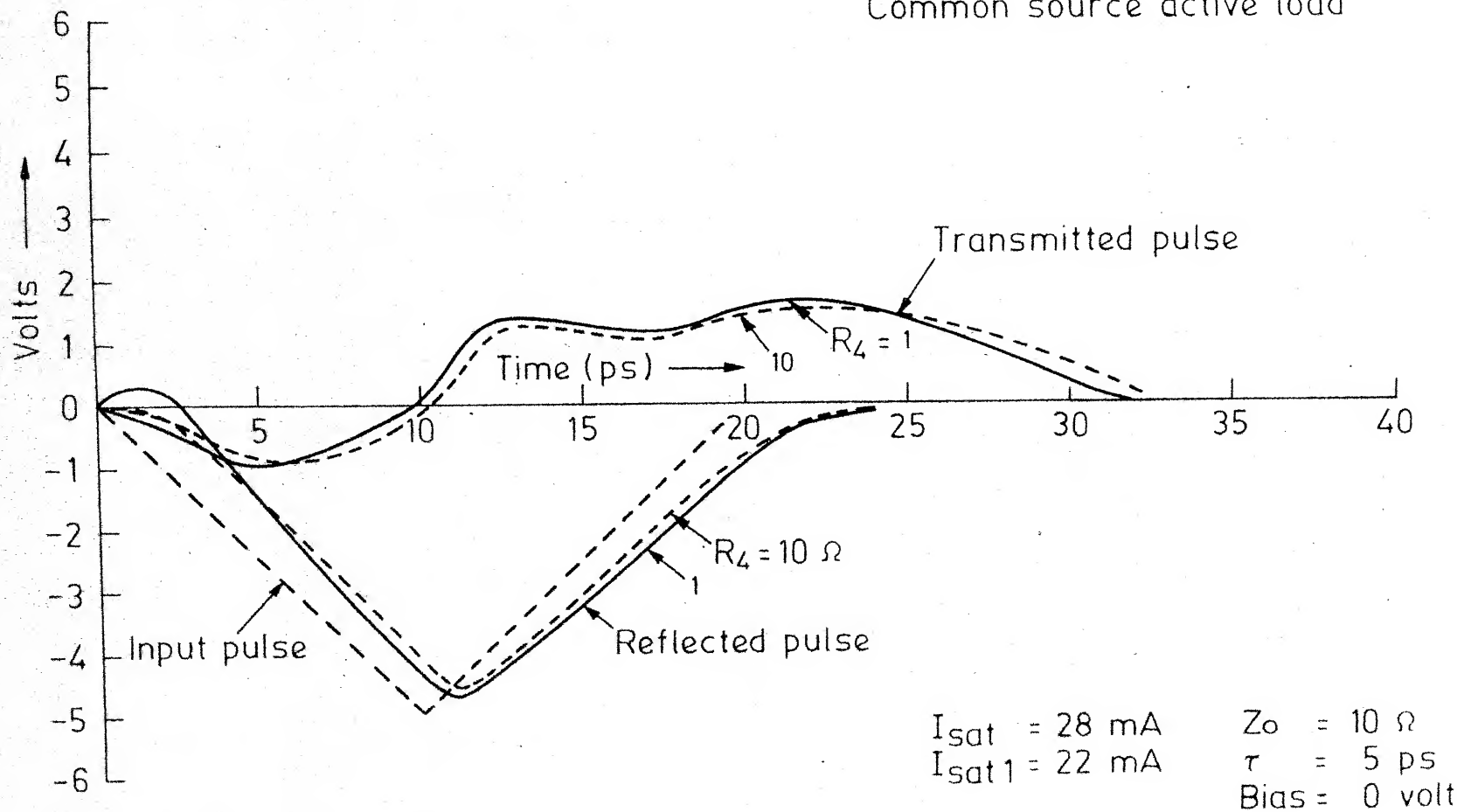


Fig. 5.7 - Effect of variation in the gate series resistance on a negative going pulse.

Table 5.6

Effect of gate series resistance on a negative going pulse

R_4 (ohms)	Delay (ps)	Amplitude (volts)	Rise time (ps)
Transmitted			
10	6.6	1.45	8.6
1	6.2	1.6	9.1
Reflected			
10	1.4	4.45	7.2
1	1.2	4.65	5.6

Effect of Intrinsic Delay in MESFET

Effect of change in the intrinsic delay in the MESFET is shown in Fig. 5.8 and 5.9 for positive and negative going pulse respectively. As seen from these figures, there is hardly any change in the reflected pulses when the intrinsic delay τ varies from 0.125 ps to 10 ps. Of course the delay in the transmitted pulses increases when the intrinsic delay in the transistor is increased. These results are summarized in Table 5.7.

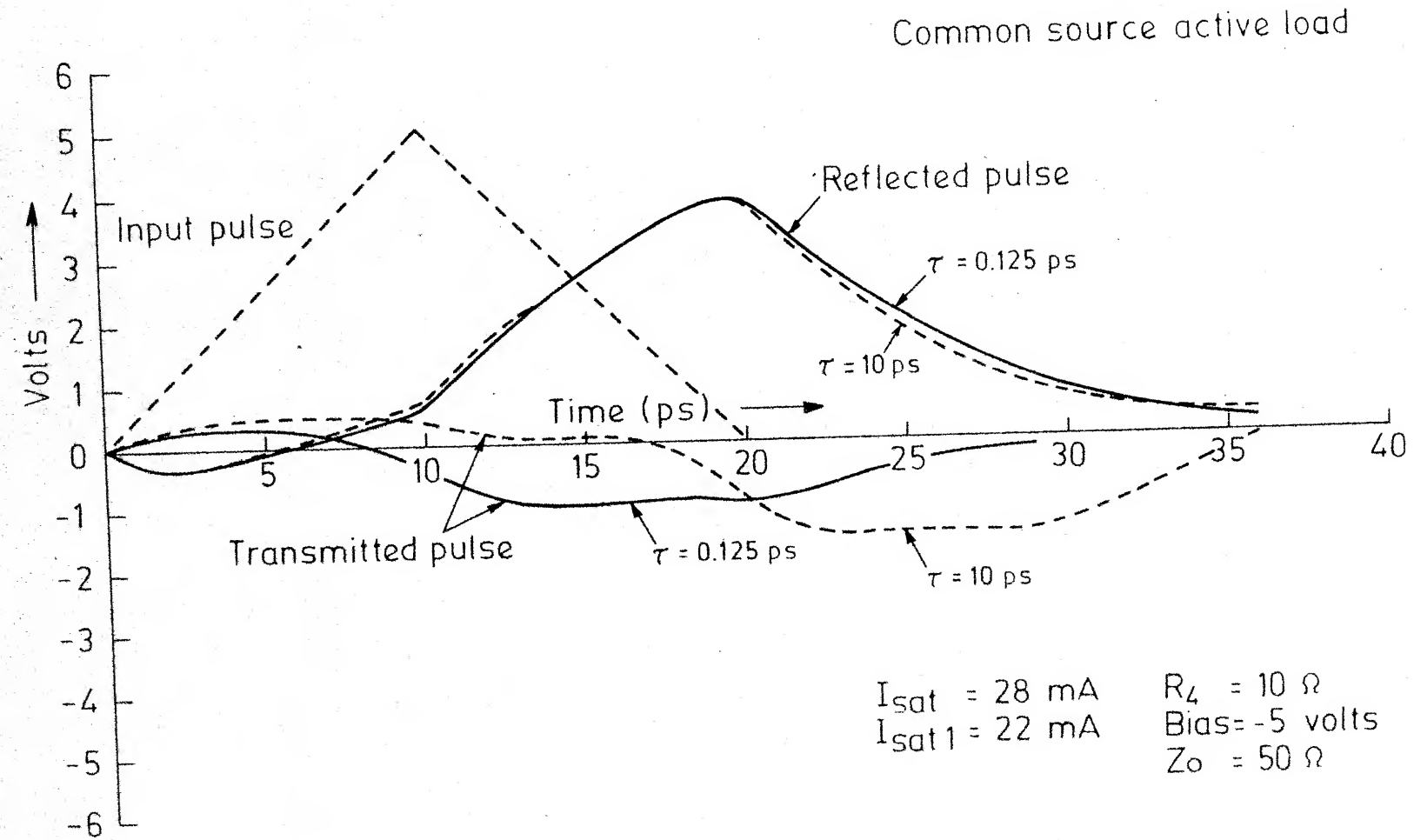


Fig. 5.8- Effect of variation in intrinsic transistor delay on a positive going pulse.

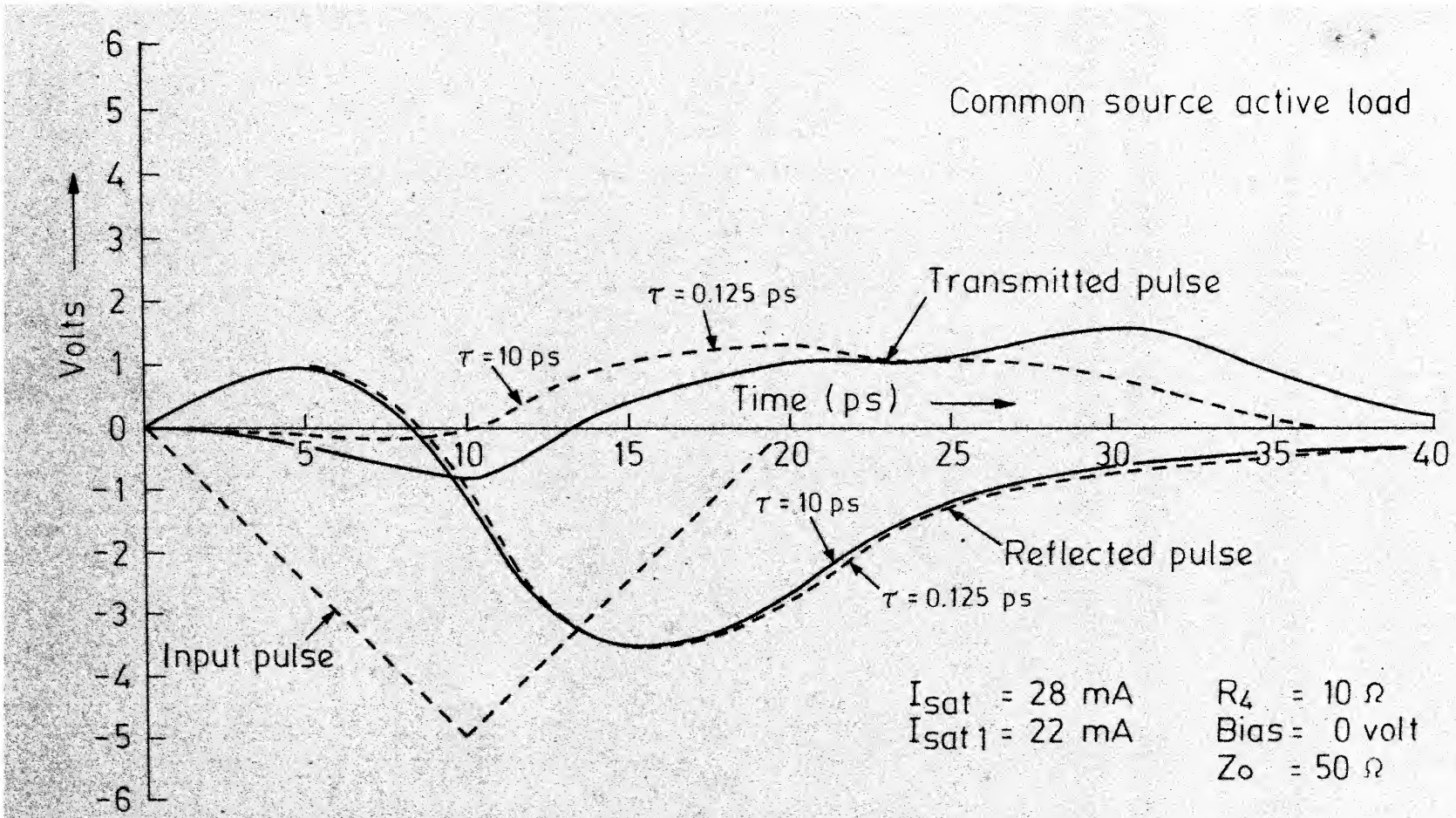


Fig. 5.9 - Effect of variation in intrinsic transistor delay on a negative going pulse.

Table 5.7

Effect of intrinsic transistor delay

Pulse type	Intrinsic delay (ps)	Pulse delay (ps)
Transmitted Pulse		
Positive going	0.125	5.4
Positive going	10	14.6
Negative going	0.125	7.7
Negative going	10	13

Chapter 6

SOURCE FOLLOWER PULSE AMPLIFIER CONFIGURATION

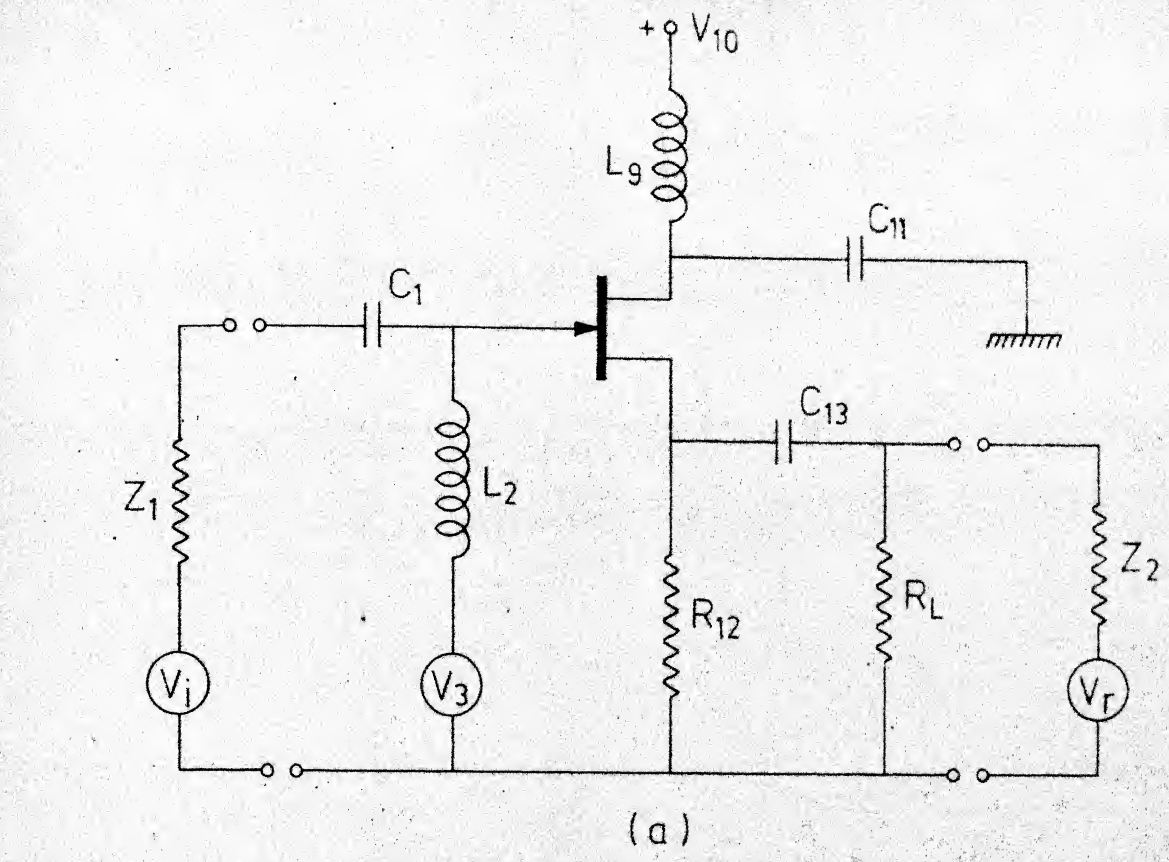
6.1 Transient Analysis

In logic gate circuits the source follower pulse amplifiers are used as an output driver circuit [14] [redacted]. This output driver also greatly enhances the logic gates ability to drive other circuits with a minimal increase in propagation delay. In fact, a low output impedance, such as that provided by the output driver circuit, is an absolute necessity for maximum speed to be achieved in a practical logic system. The price paid for this high speed capability is increased power consumptions.

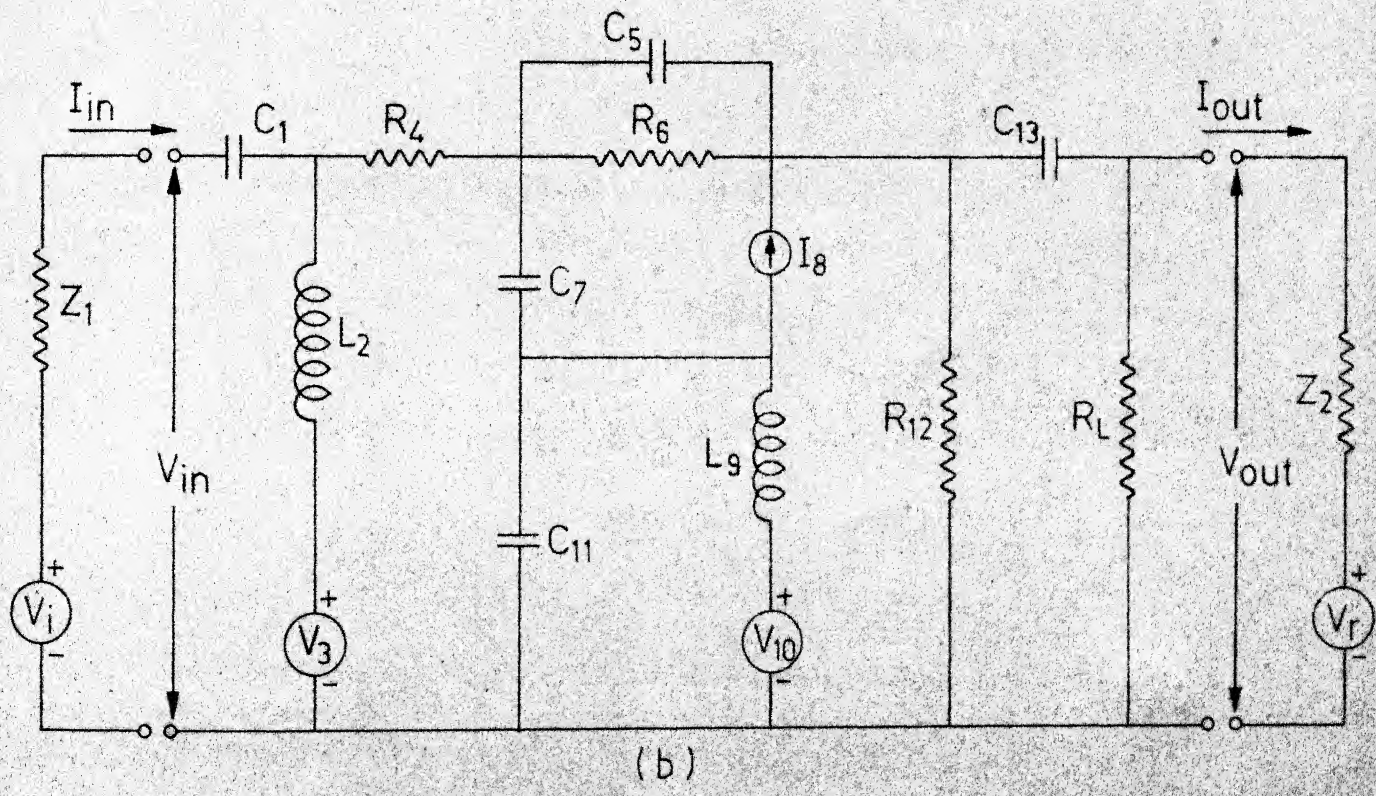
In this analysis we consider only the basic circuit as shown in Fig. 6.1(a) where inductors (L_2 and L_9) are used for biasing the circuit. Capacitors C_1, C_{11} and C_{13} are used for bypassing the a.c. The equivalent circuit is shown in Fig. 6.1(b). The aim of this analysis is to study how the circuit and device parameters effect the transmitted and reflected pulses.

For transient analysis, the voltages across capacitors and the currents in inductors are taken as state variables.

As before first two parameters V_i and V_r are defined, and used in the transmission line transient analysis, as follows :



(a)



(b)

Fig. 6.1 - MESFET in source follower configuration with biasing network and input - output transmission line equivalent circuit.

$$V_i = V_{in} - Z_1 I_{in} \tag{6.1}$$

$$V_r = V_{out} - Z_2 I_{out} \tag{6.2}$$

where Z_1 is the impedance of the input line and Z_2 is the impedance of the output line. The sign convention is same as used in Sec. 4.1.

The input and output currents can be expressed in terms of state variables as

$$I_{in} = C_1 \frac{dV_1}{dt} \tag{6.3}$$

$$I_{out} = C_{13} \frac{dV_{13}}{dt}\left(\frac{R_L}{R_L+Z_2}\right) - \frac{V_r}{R_L+Z_2} \tag{6.4}$$

These relations alongwith (6.1) and (6.2) are used to calculate V_{in} and V_{out}.

Derivatives of the state variables used for updating the values of the state variables are derived by writing circuit equations based on Kirchoff's laws. These may be written as

$$\frac{dV_1}{dt} = I_1/C_1 \tag{6.5}$$

$$\frac{dI_2}{dt} = V_2/L_2 \tag{6.6}$$

$$\frac{dV_7}{dt} = I_7/C_7 \tag{6.7}$$

$$\frac{dV_5}{dt} = I_5/C_5 \tag{6.8}$$

$$\frac{dI_9}{dt} = V_9/L_9 \tag{6.9}$$

$$\frac{dV_{13}}{dt} = I_{13}/C_{13} \tag{6.10}$$

$$\frac{dV_{11}}{dt} = I_{11}/C_{11} \tag{6.11}$$

The variables I_1, V_2, I_5, I_7, V_9, I_{11} and I_{13} are given by the following relations,

$$K_R = R_L/(Z_2 + R_L)$$

$$I_{13} = (V_7 + V_{11} - V_5 - V_{13} - V_o K_R)/(Z_2 K_R) \tag{6.12}$$

$$I_1 = (V_I - V_1 + I_2 R_4 - V_7 - V_{11})/(Z_1 + R_4) \tag{6.13}$$

$$I_7 = I_1 - I_2 + I_8(t) - (V_7 + V_{11} - V_5 + I_{13}R_{12})/R_{12} \tag{6.14}$$

$$I_5 = I_1 - (I_2 + I_7 + V_5/R_6) \tag{6.15}$$

$$I_{11} = I_7 - (I_9 + I_8(t)) \tag{6.16}$$

$$V_2 = V_I - (Z_1 I_1 + V_1 + V_3) \tag{6.17}$$

$$V_9 = V_{11} - V_{10} \tag{6.18}$$

D.C. Analysis

Initialization of state variables is done by d.c. analysis of the circuit shown in Fig. 6.1(b). The current I_8 at d.c. condition is found as follows.

Considering a value of I_8 ($I_8 = X$) the gate to source bias is

$$V_{GS} = V_3 + V_B - X R_L$$

For $V_{10} - V_{GS} + V_B \rangle V_P$,

$$X = I_{SAT}[1 - 3((V_3 + V_B - X R_L)/V_P) + 2 (V_3+V_B-XR_L)/V_P] \qquad (6.19)$$

For

$$(V_{10} - V_{GS} + V_B) < V_P$$

$$X = A[V_{10} - B[(V_{10} - V_3 + V_B)^{3/2} - (V_B - V_3)^{3/2}]] \qquad (6.20)$$

For getting a large value of g_m the biasing should be such that the circuit is in active region, i.e., it should satisfy the first condition. The root of the equation (6.19) in the selected region in V-I curve is the solution of I_8. Other d.c. equations used are given below.

$$V_5 = R_6(V_3 + I_8R_L)/ \quad (R_6 + R_4 + R_L)$$

$$V_1 = -V_3$$

$$V_{11} = V_{10}$$

$$I_9 = -I_8$$

$$I_2 = -V_5/R_6$$

$$V_{13} = V_3 + I_2R_4 - V_5$$

$$V_7 = V_3 + I_2R_4 - V_{10}$$

The listing of the program developed for analysing this circuit is attached in the Appendix II.

6.2 Results

The circuit configuration analysed is shown in Fig. 6.1. A uniform transmission line section of length L is connected at the input and the output is terminated by a load resistor R_L. Considerations regarding the length of the transmission line, the source resistance R_s and the shape of the input pulse remain the same as considered in Section 4.2.

The MESFET characteristics used correspond to the measured d.c. characteristics of a Plessey GAT3 field effect transistor in a microstrip package. For other elements of the MESFET equivalent circuit, typical guessed values have been used and may not correspond to actual values of GAT3. Referring to Fig. 6.1, various values used in the computer simulation are

$C_1 = C_{13} = 120$ pF

$L_2 = L_9 = 0.5$ nH

$R_4 = 10$ ohms

$C_o = 0.4$ pF

$V_b = 0.1$ volt

$I_s = 1$ nA

$T = 300^{\circ}K$

C_7 = 0.02 pF

I_{sat} = 28 mA

τ = 5 p sec.

V_p = 5.1 V

A = 16.14×10^{-3}

B = 0.2924

R_L = 10 K Ohms

R_{12} = 50 Ohms

C_{11} = 4 X C_1

V_{10} = 10V

Computer simulation has been carried out to study effects of the variations in the following parameters.

i) Gate bias

ii) Characteristic impedance of the input line

iii) Gate series resistance R_4, and

iv) The intrinsic delay in the transistor τ

The main results of this analysis are summarized in the following paragraphs. For all these simulations, triangular input pulses with rise time and fall time of 10 pico second and peak amplitude of 5 volts have been considered. Both the positive going and negative going pulses have been studied. The results shown in Figs. 6.2 through 6.9 depict the incident and reflected voltage waveforms at the MESFET input and the output voltage waveform across the load resistance R_L.

(i) Effect of impedance of the input line

Effect of variation in the characteristic impedance of the transmission line connected at the input for a source follower circuit is shown in Fig. 6.2 and 6.3 for positive and negative going pulses respectively. The main observations from Fig. 6.2 and 6.3 are summarized in Table 6.1 and 6.2 respectively. The characteristic impedance of the input line (Z_o) along with gate series resistance (R_4) determines the charging gate to source capacitance (C_5) and gate to drain capacitance (C_7). As the charging time of the capacitors increases with the increase of Z_o, the delay for both transmitted and reflected pulses increases with the increase in impedance level. The initial negative portion of the reflected pulse for high impedance level (150 ohms) is present in this circuit also. This cause is the same as given in Sec. 4.2. Another interesting feature of these results is that the transmitted pulses start appearing at the same instant with the input pulse though there is 5 ps intrinsic delay in the transistor. The cause of this perhaps can be explained as follows. The feedback capacitance C_5 (Fig. 6.1) is evaluated from the following relation.

$$C_5 = C_o/\sqrt{1 - V_5/V_B}$$

where

$$C_o = 0.4 \text{ pF} \; ; \; V_B = 0.1 \text{ V}$$

and $0 \ll V_5 \ll -5$ V.

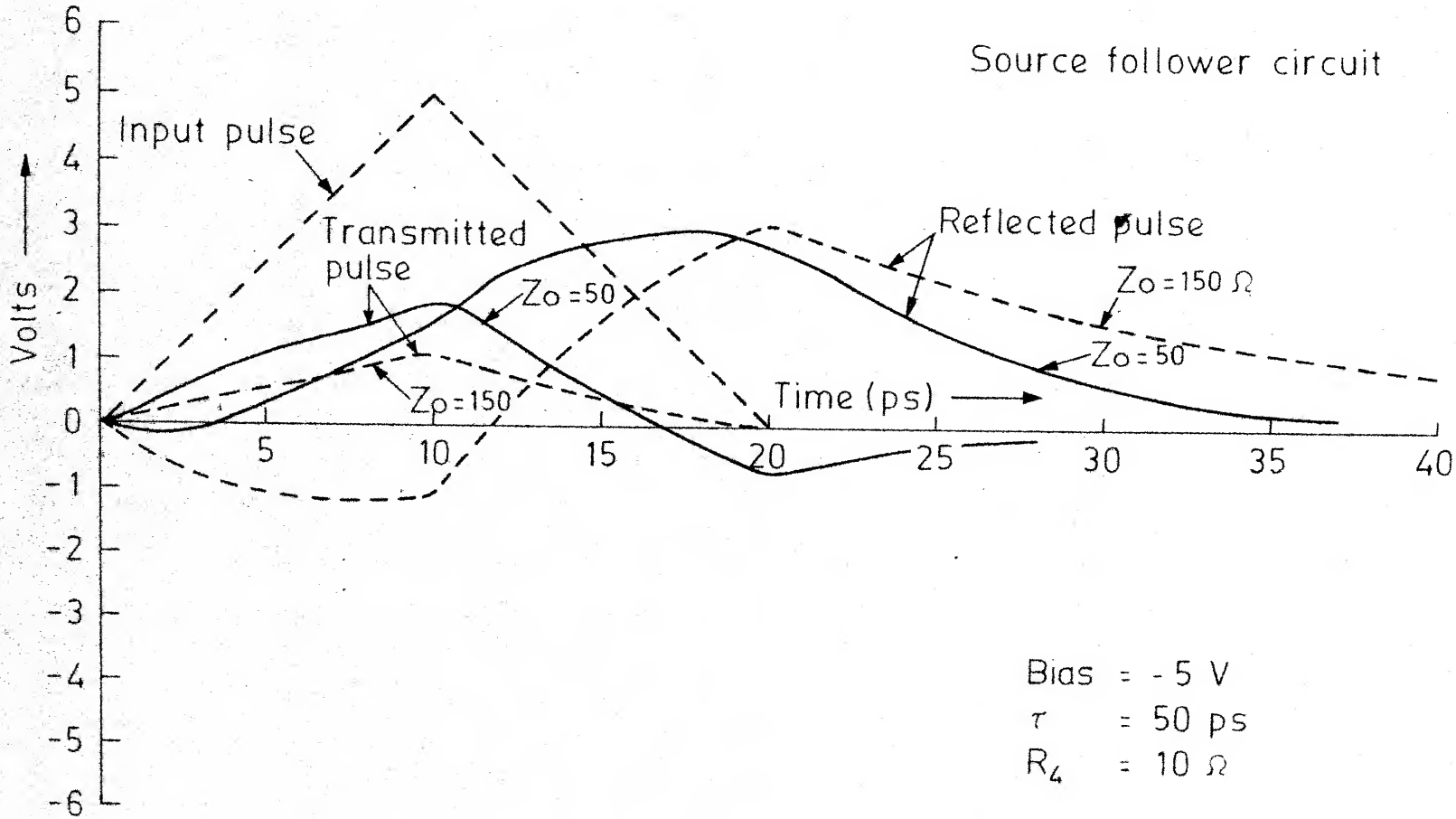


Fig. 6.2 - Effect of variation in input line on a positive going pulse.

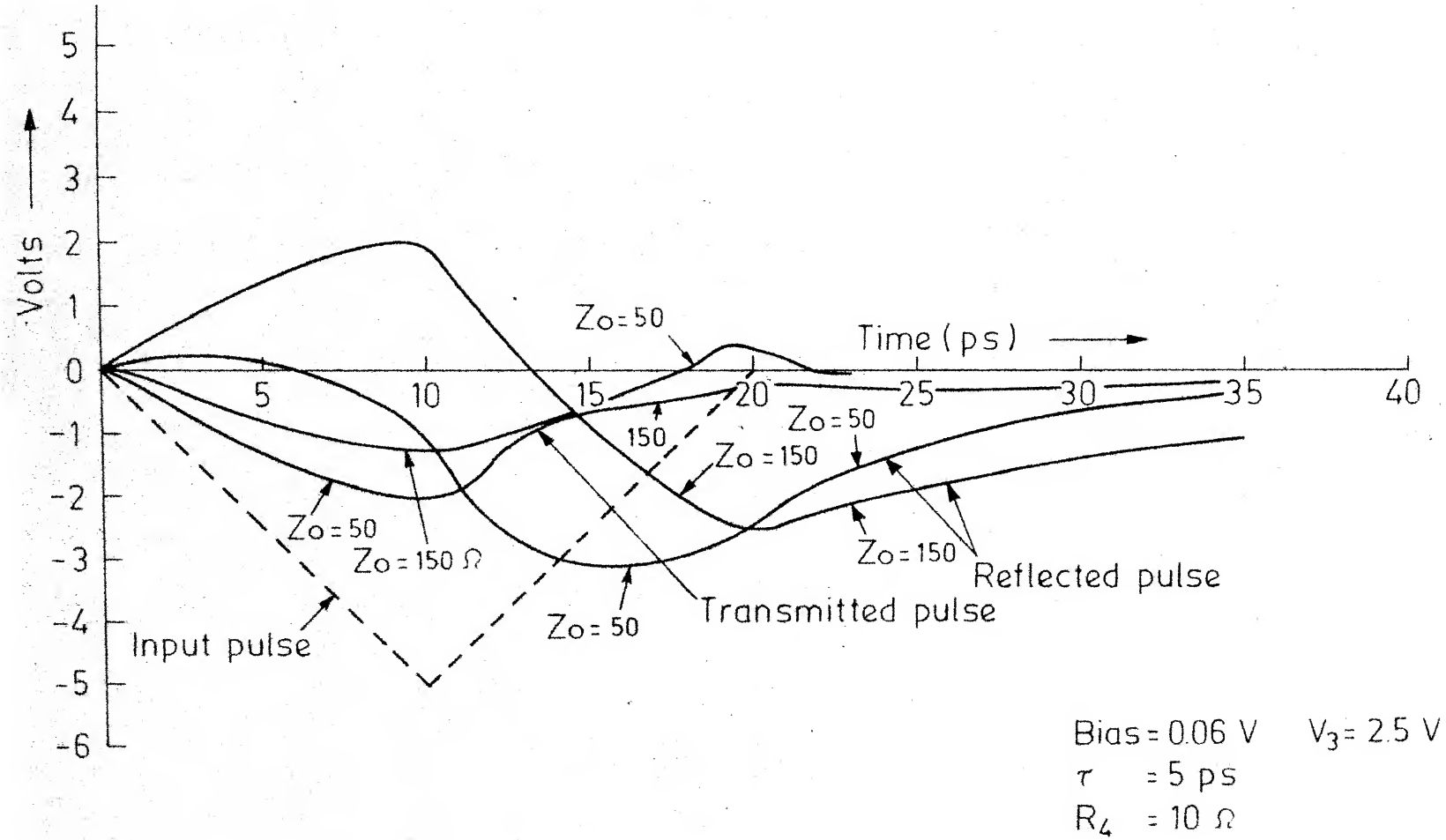


Fig. 6 3 - Effect of variation in input line impedance on a negative going pulse

The value of C_7 is taken constant and is equal to 0.2 pF.

So,

$$2.5 < \frac{C_5}{C_7} < 6.5$$

C_7 which is the feedback capacitance for common source amplifier is much smaller than the feedback capacitance for source follower circuit. Again the input and transmitted voltages are in the same phase for a source follower circuit. The numerical calculation yields that the magnitude of leakage current through the feedback capacitor for a source follower circuit is comparable with the drain current. Initial portion of the transmitted pulses is perhaps because of this leakage current.

Table 6.1

Effect of input line impedance on a positive going pulse

Impedance (ohms)	Delay (ps)	Amplitude (volts)	Rise time (ps)
Transmitted pulse			
50	-0.6	1.9	8.1
150	0.4	1.1	7.8
Reflected pulse			
50	4.8	3.0	9.2
150	10	3.1	6.25

Table 6.2

Effect of input line impedance on a negative going pulse

Impedance (ohms)	Delay (ps)	Amplitude (volts)	Rise time (ps)
Transmitted pulse			
50	-1.2	2.1	6.7
150	-0.4	1.3	7.5
Reflected pulse			
50	5.6	3.2	5.9
150	11	2.6	5.2

From the results tabulated in Table 6.1 and 6.2 it can be concluded that low input impedance line is favourable for this circuit also.

i)Effect of Variation in Gate Bias Voltage

Effect of gate bias on transmitted and reflected pulse for a source follower circuit is shown in Fig. 6.4 and 6.5 for positive and negative going pulses, respectively. The main results from Fig. 6.4 and 6.5 are summarized in Table 6.2 and 6.3. There is no delay in the transmitted pulse as discussed in previous section. Due to high leakage current which can only be effected by the input line impedance, the change of drain current due to change in bias can not effect the

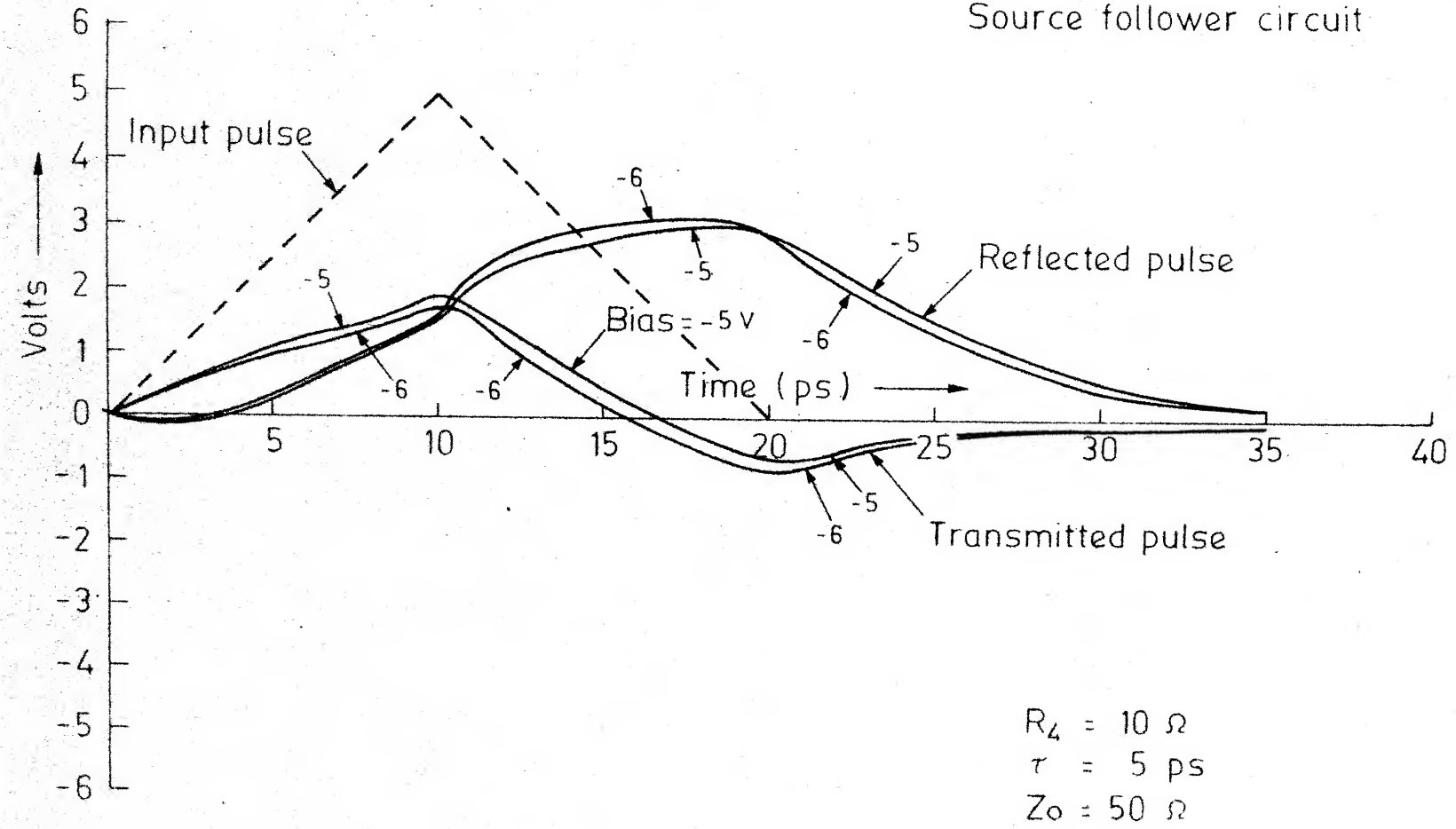


Fig. 6.4 - Effect of gate bias variation on a positive going pulse.

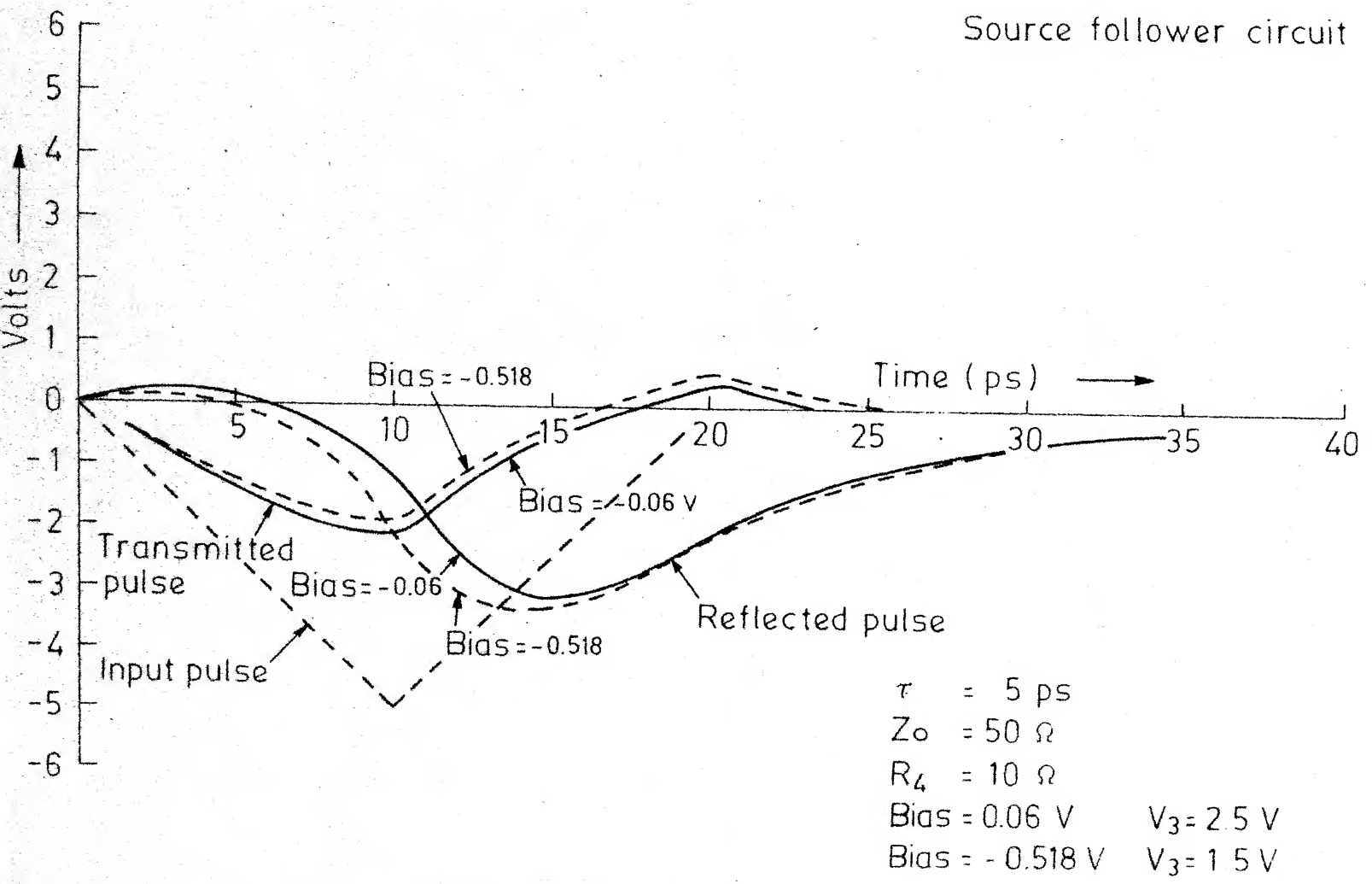


Fig. 6.5 - Effect of gate bias variation on a negative going pulse.

transmitted pulse much. For a positive input pulse the change in bias does not effect the transmitted pulse except the amplitude which decreases as the bias goes beyond cut-off But rise time and delay improve slightly as the bias changes from -5V to -6V. For a negative input pulse, the rise time of the transmitted pulse increases as the bias changes from -0.06 V to -0.518 V. In this case, both the delay and rise time of the reflected pulse decreases as the bias goes more negative.

Table 6.3

Effect of bias level on a positive going pulse

Bias (volts)	Delay (ps)	Amplitude (volts)	Rise time (ps)
Transmitted pulse			
-5	-0.6	1.9	8
-6	-0.6	1.72	7.9
Reflected pulse			
-5	5	2.95	9.4
-6	4.8	3.1	8.2

(iii) Effect of Gate Series Resistance

Effect of variations in the value of series resistance of the gate junction is shown in Fig. 6.6 and 6.7 for positive

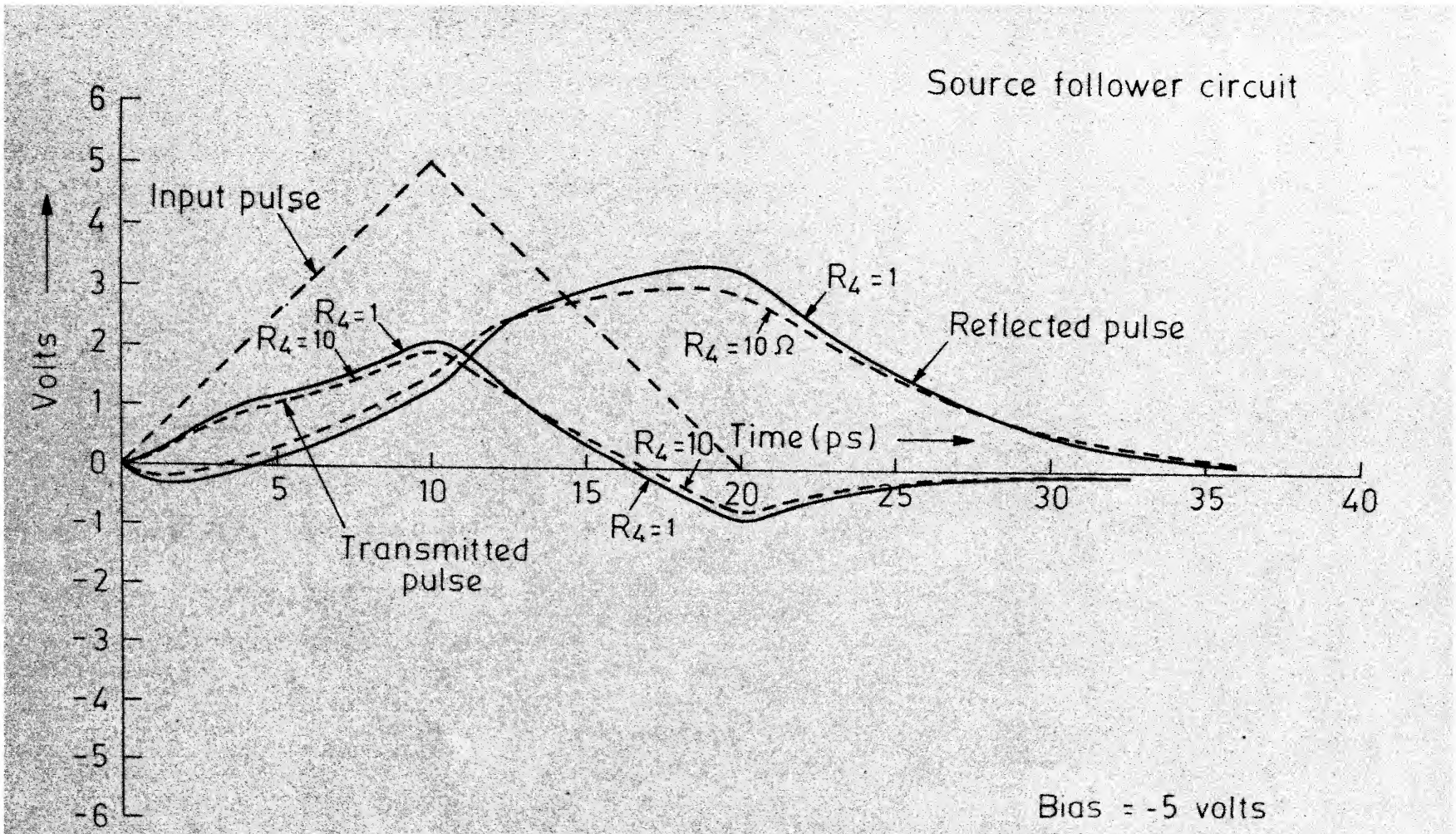


Fig. 6.6 - Effect of variation in the gate series resistance on a positive going pulse

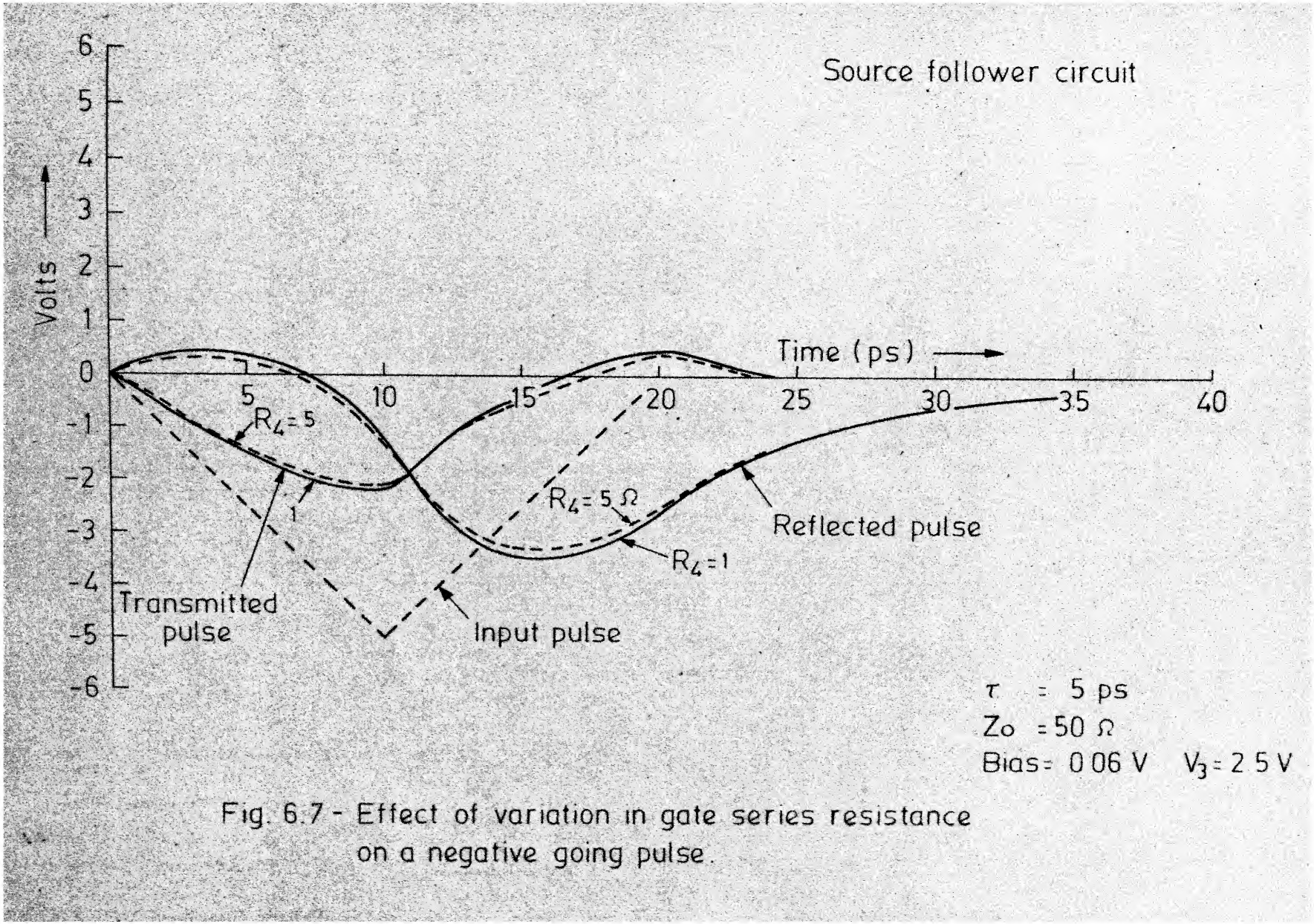


Fig. 6.7 - Effect of variation in gate series resistance on a negative going pulse.

Table 6.4

Effect of bias level on a negative going pulse

Bias (volts)	Delay (ps)	Amplitude (volts)	Rise time (ps)
Transmitted pulse			
-0.06	-1.2	2.1	6.7
-0.518	-1.3	1.95	7.6
Reflected pulse			
-0.06	5.6	3.2	5.9
-0.518	4.5	3.35	4.9

and negative going pulses respectively. The aim of this study is to find out whether the value of this resistance is critical for the operation of MESFET as a source follower pulse amplifier. The value of R_4 selected for circuit simulation are 1.0, 5.0 and 10.0 ohms. But the change in transmitted and reflected pulses is very insignificant. Figures are drawn only for two values of R_4. As the results for R_4 equal to 10 ohms are already tabulated in Table 6.1 ($Z_o = 50$), the results for R_4 equal to 1 and 5 ohms are not tabulated. The change of R_4 is not significant because the input capacitance (C_7) for source follower circuit has a very

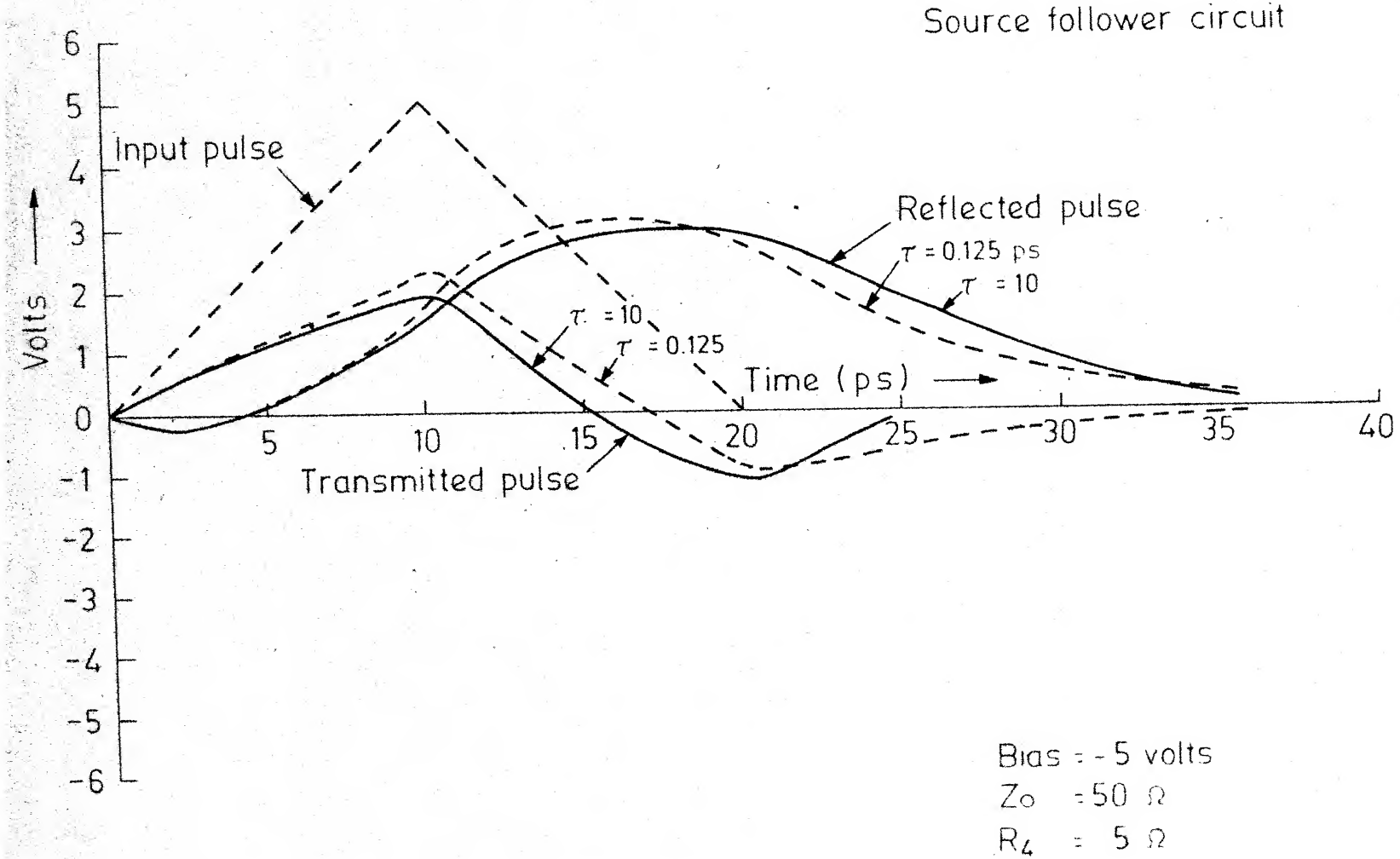


Fig 6.8 - Effect of variation in intrinsic transistor delay on a positive going pulse

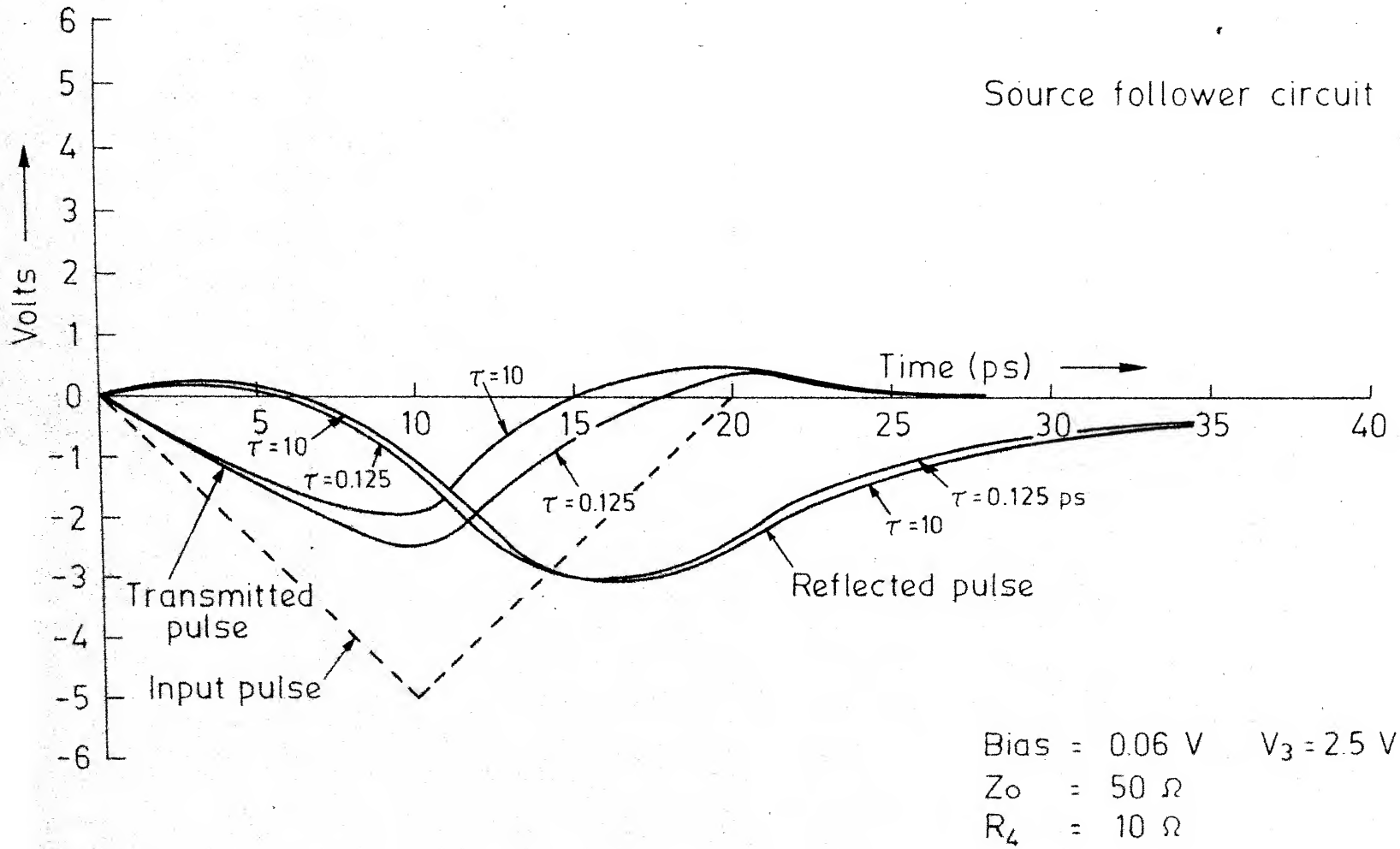


Fig. 6.9 - Effect of variation in intrinsic transistor delay on a negative going pulse.

low value and therefore provides a very high input impedance. The input line impedance is taken 50 ohms which is also very large compared to R_4. The value of Z_o can not taken low (say 10 ohms) because that increases the leakage current heavily and large amount of charge accumulates in C_5 and C_7. This increases the discharging time of the capacitors, and the fall time for both transmitted and reflected pulse is increased by large amount. So it can be concluded that with the given circuit parameters the change in R_4 is not significant both for transmitted and the reflected pulses.

Effect of Intrinsic Delay in MESFET

Effects of changes in the intrinsic delay in MESFET are shown in Fig. 6.8 and 6.9 for positive and negative going pulses respectively. As seen from these figures, there is hardly any change in either transmitted or reflected pulses when the intrinsic delay τ is varied from 0.125 ps to 10 ps. High leakage current in the source follower circuit is responsible for this phenomena. Results for τ equal to 5 ps are tabulated in Table 6.1.

Chapter 7

SOURCE FOLLOWER PULSE AMPLIFIER WITH ACTIVE LOAD

7.1 Transient Analysis

Source follower with active load[14] is generally used as output driver circuit in MESFET logic, and is discussed in Sec. 6.1. Active load used in the source follower circuit improves the rise time and fall time of the transmitted pulse by causing charging and discharging of capacitors through the active load.

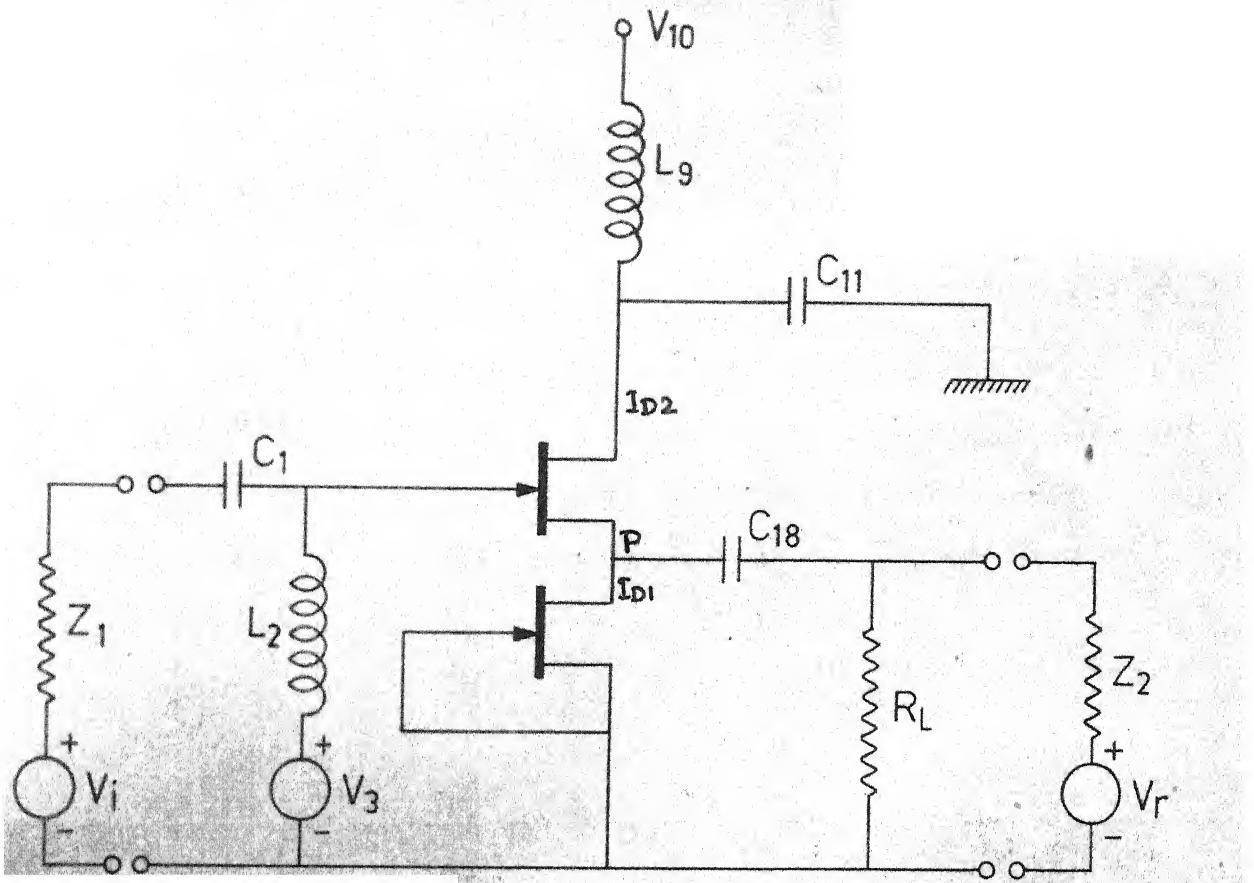
The equivalent circuit along with biasing network considered for the present analysis is shown in Fig. 7.1. The two transmission lines connected at input and output have characteristic impedance Z_1 and Z_2 respectively.

Two parameters V_i and V_r are defined for convenience in transient analysis of transmission line and can be written as follows.

$$V_i = V_{in} + Z_1 I_{in} \tag{7.1}$$

$$V_r = V_{out} - Z_1 I_{out} \tag{7.2}$$

where I_{in} and I_{out} are input and output currents and V_{in} and V_{out} are input and output voltages respectively. All other considerations regarding the Sign convention, Z_1, Z_2 and R_L remain same as used Section 4.1. The capacitors C_1



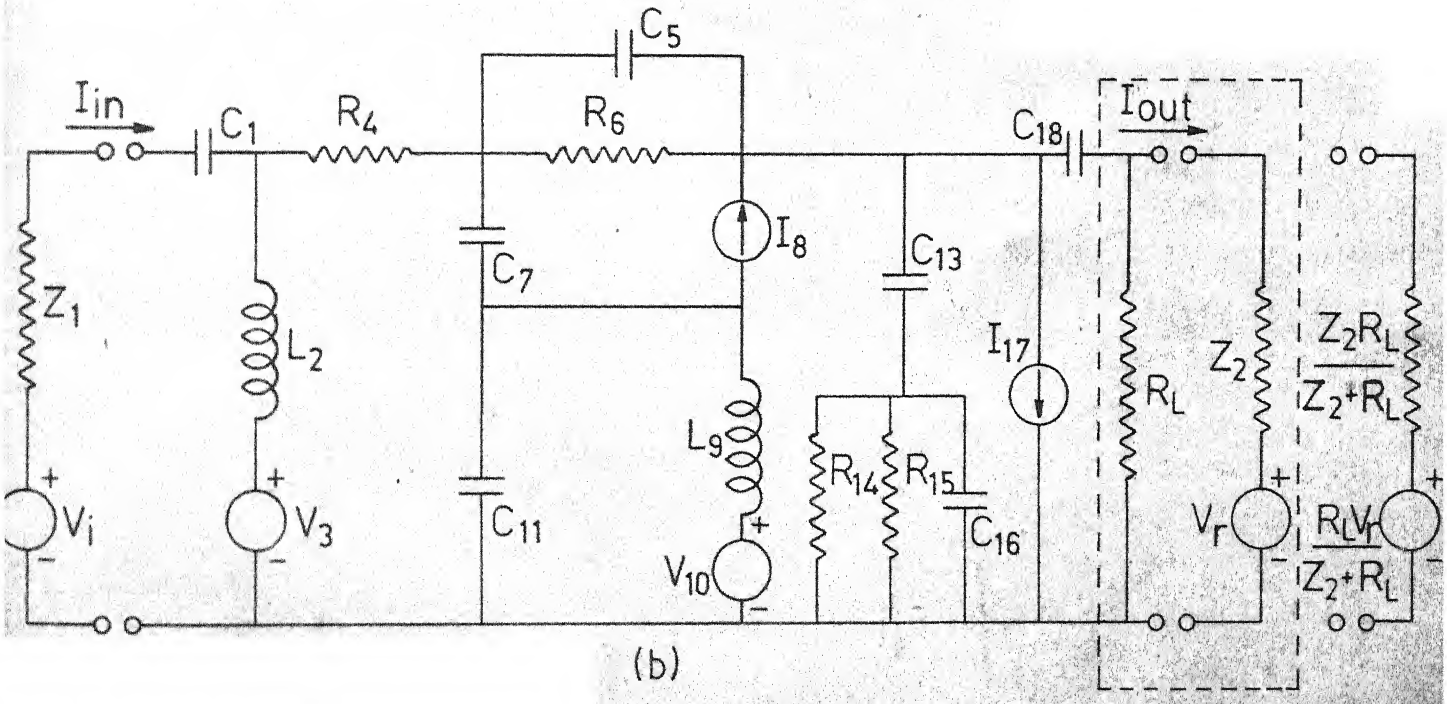


Fig. 7.1 - MESFET in source follower with active load configuration with biasing network and input - output transmission line equivalent circuit.

and C_{18} are used to block the d.c. voltages from input and output signals. The inductors L_2 and L_9 are used for blocking the R.F. signals from bias sources. C_{11} gives an a.c. path to the output signal. Proceeding in a similar way as is done in Section 4.1 and assuming voltage across capacitors and current through inductors as state variables, the input and output currents can be expressed in terms of state variables as :

$$I_{in} = C_1 \frac{dV_1}{dt} \tag{7.3}$$

$$I_{out} = C_{18} \frac{dV_{18}}{dt}\left(\frac{R_L}{R_L+Z_2}\right) - \frac{V_r}{R_L+Z_2} \tag{7.4}$$

These relations alongwith equations (7.1) and (7.2) determine V_{in} and V_{out}. The derivatives of the state variables can be expressed by the following relations.

$$\frac{dV_{18}}{dt} = \frac{I_{18}}{C_{18}} \tag{7.5}$$

$$\frac{dV_{16}}{dt} = \frac{I_{16}}{C_{16}} \tag{7.6}$$

$$\frac{dV_{13}}{dt} = \frac{I_{13}}{C_{13}} \tag{7.7}$$

$$\frac{dV_{11}}{dt} = \frac{I_{11}}{C_{11}} \tag{7.8}$$

$$\frac{dI_9}{dt} = \frac{V_9}{L_9} \tag{7.9}$$

$$\frac{dV_7}{dt} = \frac{I_7}{C_7} \tag{7.10}$$

$$\frac{dV_5}{dt} = \frac{I_5}{C_5} \tag{7.11}$$

$$\frac{dI_2}{dt} = \frac{V_2}{L_2} \tag{7.12}$$

$$\frac{dV_1}{dt} = \frac{I_1}{C_1} \tag{7.13}$$

The variables I_1, V_2, I_5, I_7, V_9, I_{11}, I_{13}, I_{16} and I_{18} are given by the following relations :

Let $K_p = R_L/(Z_2 + R_L)$.

$$I_{18} = (V_{13} + V_{16} - V_{18} - V_r K_p)/(Z_2 K_p) \tag{7.14}$$

$$I_{13} = (V_7 + V_{11} - V_5 - V_{13} + I_{16} R_k)/R_k \tag{7.15}$$

$$I_{16} = I_{13} - V_{16}/R_k \tag{7.16}$$

$$I_7 = I_1 - I_2 + I_8 - I_{13} - I_{17} - I_{18} \tag{7.17}$$

$$I_1 = (V_I - V_1 + I_2 R_4 - V_7 - V_{11})/(Z_1 + R_4) \tag{7.18}$$

$$V_2 = V_I - (Z_1 I_1 + V_1 + V_3) \tag{7.19}$$

$$I_5 = I_1 - I_2 - I_7 - V_5/R_6 \tag{7.20}$$

$$V_9 = V_{11} - V_{10} \tag{7.21}$$

$$I_{11} = I_7 - I_9 - I_8 \tag{7.22}$$

Initial values of state variables are found out by d.c. analysis of the circuit. All the currents and voltages at d.c. condition become known if the voltage V_x at ethe point P can be found out for which $I_{D1} = I_{D2}$ (see Fig.7.1). Let $I_D(1)$ is the current through amplifier transistor and $I_D(2)$ is the current through load transistor. $I_D(1)$ and $I_D(2)$ can be calculated by assuming a value of V_x. If a function $F(V_x)$ can be written as,

$$F(V_x) = I_D(1) - I_D(2)$$

the root of the equation $F(V_x) = 0$ is the solution for V_x. By choosing a suitable zone in the characteristic curve one can select two values of V_x for which $F(V_x)$ changes sign. Then by using bisection method the root can be found out. The complete study of this problem needs much omputational time and has not been undertaken here.

Chapter 8

CONCLUDING REMARKS

8.1 Important Results

One of the significant results of the computer simulation for MESFET amplifiers is the realization of the fact that there is a substantial reflection of the incident pulse at the input terminals. Magnitude of the reflected pulse is comparable with input and transmitted pulse in all the three configurations analysed. So the presence of this reflected pulse should be considered in the sub-system design. The input circuit of the common source pulse amplifier and that of common source pulse amplifier with active load are practically the same. So the reflected pulse waveforms for the above two cases are almost identical. In the common source circuit a clamping of reflected pulse is observed for a positive going pulse when the line impedance is low. This reduces the rise time. For a source follower circuit a low impedance line is not favourable because of the larger value of source-to-gate capacitance as compared with drain-to-gate capacitance in the previous case. This has been discussed in Sec. 6.2. The delay in reflected pulse depends mainly on the input capacitance and the impedance of the feeding line. The reflection loss (reduction in amplitude of the reflected

pulse) depends upon the resistance associated with the input gate-source schottky barrier junction.

For a positive going input pulse in a common source configuration there is considerable reduction in rise time of the transmitted pulse when clamping occurs in the circuit. A negative going pulse cannot be sharpened by clamping because of pinch-off at negative gate voltage. Reduction of rise time of the transmitted pulse for a negative going pulse can be achieved by reducing the input line impedance.

The conclusions regarding transmitted pulse that are drawn for common source pulse amplifier are valid for pulse amplifier with active load also. However in this case the dealy time increases slightly. As discussed in Sec. 5.2 this increase in delay is due to the nonlinearity in active load. But one main advantage in the active load circuit is sharp reduction in fall time of the transmitted pulse.

Because of high current through the feedback capacitor the changes in transmitted pulse with change in parameters R_4, τ and gate bias are not very prominent in the source follower circuit. Thus it may be concluded that for a source follower circuit it is desirable to use MESFETs which have very low gate to source capacitance.

8.2 Suggestions for Further Work

Basic inverter gate in MESFET logic circuit is realised by using a common source pulse amplifier with active load connected with a source follower with active load. The role of these two amplifiers has been discussed earlier in Sections 5.1 and 7.1. The numerical calculation for source follower with active load configuration could not be carried out in the present work. These calculation will lead to a detailed understanding of an inverter gate in MESFET logic for picosecond pulses. In a similar manner, different logic gate circuits can be analysed. The simulation of these logic circuits is helpful for a better design of these circuits.

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```
C
C     ------------------------------------------------------------------
C     THIS  PROGRAM  CARRIES  OUT  TRANSIENT  ANALYSIS  OF  COMMON
C     SOURCE  ACTIVE  LOAD  AMPLIFIER  WITH  INPUT  OUTPUT  TR.LINE
C     SHOWN  IN  FIG. 3.1
C     SOME  OF  THE  IMPORTANT  NOTATIONS  ARE  EXPLAINED  BELOW.
C     THE  MAIN  PROGRAM  CARRIES  MAINLY  THE  TRANSIENT  ANALYSIS  OF
C     TRANSMISSION  LINE.
C     ZA - CHARACTERISTIC  IMPEDANCE  OF  INPUT  LINE
C     LA - NUMBER OF  SEGMENTS  IN  INPUT  LINE. IT  DEPENDS  ON  THE
C     ELECTRICAL  LENGTH  AND  THE  BASIC  TIME  STEP  DT  SPECFIED
C     VBI - GATE  BIAS
C     KTM - TOTAL  NO  OF  TIME  STEPS  IN  TRANSIENT  ANALYSIS
C     PA - PULSE  AMPLITUDE  AT  THE  GENERATOR
C     VINC - VOLTAGE  VARIABLES  FOR  TRANSMISSION  LINE  ANALYSIS
C     VREF - VOLTAGE  VARIABLES  FOR  TRANSMISSION  LINE  ANALYSIS
C     VS - VOLTAGE  OF  THE  INPUT  PULSE  AT  THE  GENERATOR
C     ------------------------------------------------------------------
      DIMENSION VINC([illegible],2),VREF(402,2),VS(1000),E(305),F(305),C(305)
     2,D([illegible])
      DOUBLE PRECISION ZA,VBI,PA,RL,VINC,VREF,VS,VI,VO,RT,IIN,IOUT,V,VL
     2,A,B,ISAT,[illegible],DT,TD,R4,R9,VP,C7,C12,C0,VB,C1,L2,V14,L13,C16
     3,D,E,F,A1,B1,ISAT1
      COMMON A,B,ISAT,[illegible],DT,TD,R4,R9,VP,C7,C12,C0,VB,C1,L2,V14,L13,C16
     2,A1,B1,ISAT1
C     ************************************
      READ(5,400)R4,R9,VP,C7,C12,C0
      READ(5,400)VB,C1,L2,V14,L13,C16
      READ(5,400)IS,[illegible],RL
  400 FORMAT([illegible])
C     ************************************
C *** CONTROL  PARAMETERS
C     ************************************
      [illegible]=1.E-12
      IS[illegible]=[illegible]
      ISA[illegible]=[illegible]
      R[illegible]=[illegible]
      VB[illegible]=[illegible]
C     ************************************
      CALL AB(VP,[illegible]SAT,A,B,VB)
      CALL AB(VP,ISAT1,A1,B1,VBI)
      [illegible]
      WRITE(6,[illegible])
  308 FORMAT([illegible]4X,'CALCULATION FOR NEGATIVE INPUT PULSE')
      WRITE(6,313)
  313 FORMAT([illegible]X,'COMMON SOURCE ACTIVE LOAD')
      WRITE(6,309)
  309 FORMAT(24X,[illegible]/)
      READ(5,[illegible])KTM,L
  310 FORMAT([illegible])
      V = [illegible]
      WRITE(6,311)
  311 FORMAT(/,[illegible]X,91('*'),/)
      WRITE(6,[illegible])A,B,ISAT,IS,DT,RL,[illegible]
      WRITE(6,[illegible])VB,C1,L2,V14,L13,C16,B1
      WRITE(6,[illegible])RT,R9,VP,C7,C12,C0,ISAT1
      WRITE(6,311)
```

```
  100   FORMAT(6D11.4)
  101   FORMAT(/,15X,7(3X,D11.4))
        WRITE(6,312)R4,TD,VB
  312   FORMAT(40X,*R4=*,D11.4,4X,*TD=*,D11.4,4X,*VG=*,D11.4)
        WRITE(6,311)
        K1=1
        DO 14 L=1,3
        READ(5,105)ZA
  105   FORMAT(D11.4)
        D(L)=ZA
        NS=LA+1
        PA=-10.
C          INITIAL  VAND I
        DO 1 J=1,NS
        VINC(J,1)=0.DO
    1   VREF(J,1)=0.DO
C         INPUT PULSE
C         *************************************
        DO 2 J=1,80
    2   VS(J)=FLOAT(J)*PA/80.DO
        DO 3 J=81,160
    3   VS(J)=PA*(1.DO-(FLOAT(J)-80.)/80.DO)
        DO 41 J=161,KTM
   41   VS(J)=0.DO
C         *************************************
C     TRANSIENT CALCULATIONS
        DO 4 K=1,KTM
        VINC(1,2)=VS(K)
        VREF(1,2)=VREF(2,1)
        DO 5 J=2,LA
        VINC(J,2)=VINC(J-1,1)
    5   VREF(J,2)=VREF(J+1,1)
        VINC(NS,2)=VINC(LA,1)
        V1=VINC(1,2)
        CALL FE*(V1,V0,K,IIN,IOUT,ZA,RL,VB1,RT)
        VREF(NS,2)=VINC(NS,2)-2.DO*IIN*ZA
        V=(VINC(1,2)+VREF(1,2))/2.DO
        VL=IOUT*RL
        DO 6 J=1,NS
        VINC(J,1)=VINC(J,2)
    6   VREF(J,1)=VREF(J,2)
        TIME=FLOAT(K)*0.125
        IF(TIME.LT.25.)GO TO 4
        IF(K.EQ.(K/3)*3) GO TO 7
        GO TO 4
    7   E(K1)=V
        F(K1)=VL
        C(K1)=TIME
        K1=K1+1
    4   CONTINUE
   14   CONTINUE
        WRITE(6,300)D(1),D(2),D(3)
  300   FORMAT(3(5X,*VALUE OF ZA =*,D11.4,13X))
        WRITE(6,301)
  301   FORMAT(1X,3(34(1H-),7X))
        WRITE(6,302)
```

```
302   FORMAT(3(2X,*VOL.AT.INP*,3X,*VOL.AT.LOAD*,4X,*TIME *,7X))
      WRITE(6,303)
303   FORMAT(3(4X,*IN VOLTS*,6X,*IN VOLTS*,6X,*SEC*,7X))
      WRITE(6,304)
304   FORMAT(3(1X,11(1H-),3X,11(1H-),4X,5(1H-),7X))
      DO 45 I=1,76
      N1=I+76
      M1=I+152
      WRITE(6,305)E(I),F(I),C(I),E(N1),F(N1),C(N1),E(M1),F(M1),C(M1)
305   FORMAT(/,3(1X,C12.5,2X,D12.5,3X,F7.2,6X))
45    CONTINUE
      STOP
      END
      SUBROUTINE FET(V1,VD,K,IIN,ICUT,Z1,Z2,V3,RL)
C     ------------------------------------------------------------------
C     AMPLIFIER IN COMMON SOURCE ACTIVE LOAD CONFIGURATION.
C     THIS SUBROUTINE CARIES OUT THE TRANSIENT ANALYSIS OF THE
C     NOTATIONS REMAIN THE SAME AS SHOWN IN THE FIG - 5.1
C     ------------------------------------------------------------------
      DOUBLE PRECISION A,B,ISAT,IS,DT,TD,R4,R5,VP,C7,C12,CO,VB,C1,L2,V1
     2,L13,C16,V14,V ,IIN,ICUT,Z1,Z2,V3,RL,VD1,ID8,ID15,I8,I13,V5,V16,V1
     3,V12,V7,I2,I13,V ,C5,C11,VD2,I16,V18,I12,RK,R6,R10,I11,I7,I1,V2,I
     4,RLP,ISAT1,A1,B1
      COMMON A,B,ISAT,IS,DT,TD,R4,R5,VP,C7,C12,CO,VB,C1,L2,V14,L13,C16
     2,A1,B1,ISAT1
      DIMENSION I8(100),I15(100)
      CALL PLUN(2000)
91    KD=(TD/DT)+1.
      IF(K.GT.1) GO TO 10
      CALL DCFET(A,B,R6,R10,VD1,R4,V14,VP,VB,ISAT,ISAT1,A1,B1,V3,ID8,V5
     2IS)
      ID15=ID8
      V16=VD1
      V11=0.
      V12=VD1-V14
      V7=VB-V16
      I2=-V3/(R4+R6)
      I13=-ID15
      V1=-V3
      C5=CO/DSQRT(1.-V5/VB)
      C11=CO/DSQRT(1.-V11/VB)
      DO 71 J=1,KD
      I8(J)=ID8
71    I15(J)=ID15
      GO TO 8
C **** TRANSIENT ANALYSIS
1     CONTINUE
      VD1=V16+(I16-ICUT)*RL
      CALL VALU(V5,VB,C5,R5,VD1,IS,ID8,CO,ISAT,VP,A,B)
      VD2=V14+V18-VD1
      CALL VALU(V11,VB,C11,R10,VD2,IS,ID15,CO,ISAT1,VP,A1,B1)
8     CONTINUE
      KM=KD-1
      DO 81 J=1,KM
      KL=KL+1-J
```

```
      I8(KL)=I8(KN)
   81 I15(KL)=I15(KN)
      I8(1)=ID8
      I15(1)=ID15
      RLP=RL/(RL+Z2)
      I16=((V9)-(V16+V7+VQ*RLP))/(Z2*RLP)
      V13=V5-(V12+V14+V11+V7)
      I12=I13+I15(KD)
      RK=R9*R10/(R9+R10)
      IF(R10.LE.0.) GO TO 19
      I11=I12-V11/RK
      GO TO 20
   19 I11=0.
   20 CONTINUE
      I7=I8(KD)+V11/RK+I16+I11-I15(KD)
      I1=((V1+I2*R4)-(V1+V5))/(Z1+R4)
      V2=V1-(Z1*I1+V1+V3)
      IF(R6.LE.0.) GO TO 15
      I5=I1-(I2+I7+V5/R6)
      GO TO 16
   15 I5=0.
   16 CONTINUE
      V16=V16+I16*(DT/C16)
      I13=I13+V13*(DT/L13)
      V11=V11+I11*(DT/C11)
      V12=V12+I12*(DT/C12)
      IF(V11.GT.VB) GO TO  21
      GO TO 22
   21 V11=VB-1.D-7
   22 CONTINUE
      V7=V7+I7* (DT/C7)
      V1=V1+I1*(DT/C1)
      I2=I2+V2*(DT/L2)
      V5=V5+I5*(DT/C5)
      IF(V5.GT.V8) GO TO 17
      GO TO 18
   17 V5=V8-1.D-7
   18 CONTINUE
      IIN=I1
      ICUT=I16*RLP-(VQ/(Z2+RL))
      RETURN
      END
      SUBROUTINE VALU(V5,VB,C5,R6,VC,IS,ID,CC,ISAT,VP,A,B)
C     ------------------------------------------------------------
C     THIS  SUBROUTINE  CARIES  OUT  THE  CALCULTION  OF  DEVICE
C     PARAMETERS
C     ------------------------------------------------------------
      DOUBLE PRECISION V5,VB,R6,VC,IS,ID,CC,ISAT,C5,VP,A,B
      IF(VC.GE.VB) GO TO 9
      C5=CC/DSQRT(1.-VC/VB)
      GO TO 10
    9 C5=CC/DSQRT(1.-VC/(VB-1.D-7))
   10 IF(V5.EQ.VB) GO TO 11
      IF(V5.LT.(-3.)) GO TO 12
      R6=(V5-VB)/(IS*(DEXP(38.7*(V5-VB))-1.))
```

```
12      R6=-V5/IS
        GO TO 13
11      R6=1./38.7/IS
13      CONTINUE
        IF(VD.LT.0.DO) GO TO 16
        IF((VD-V5+VB).GE.VB) GO TO 14
        ID=A*(VD-B*((VD-V5+VB)**1.5-(VB-V5)**1.5))
        GO TO 8
14      ID=ISAT*(1.-3.*((VB-V5)/VP)+2.*((VB-V5)/VP)**1.5)
8       CONTINUE
        GO TO 17
16      ID=0.DO
17      IF(VB.LT.(-VP+VB)) ID=0.DO
        RETURN
        END
        SUBROUTINE DCFET(A,B,R6,R10,VD1,R4,VDD,VP,VB,ISAT,ISAT1,A1,B1,V3,
       2ID,V5,IS)
C       ------------------------------------------------------------------
C       BISECTION METHOD IS FOR FINDING THE ROOT
C       THIS SUBROUTINE CARRIES OUT THE D.C ANALYSIS OF THE
C       CIRCUIT SHOWN IN FIG-9.1
C       ------------------------------------------------------------------
        DOUBLE PRECISION A,B,R10,R6,VD1,R4,VDD,VP,VB,ISAT,V3,ID,V5,X1,X2,
       2X3,FX1,FX2,FX3,IS,A1,B1,ISAT1,ID1,ID2
        CALL FLUN(2000)
        IF(V3.LE.(-5.)) GO TO 1
        IF(V3.EQ.VB) GO TO 2
        IF(V3.LT.(-3.)) GO TO 3
        R6=(V3-VB)/(IS*(DEXP(38.7*(V3-VB))-1.))
        GO TO 5
3       R6=-V3/IS
        GO TO 5
2       R6=1./38.7/IS
5       V5=V3*R6/(R4+R6)
        R10=VB/(IS*(1.-DEXP(38.7*(-VB))))
        ID1=ISAT*(1.-3.*((VB-V5)/VP)+2.*((VB-V5)/VP)**1.5)
        ID2=ISAT1*(1.-3.*(VB/VP)+2.*(VB/VP)**1.5)
        IF(ID1.GT.ID2) GO TO 60
        ID=ID1
        X1=VDD-VP+VB
        X2=VDD
        FX1=ID-A1*(VDD-X1-B1*((VDD-X1+VB)**1.5-(VB)**1.5))
50      X3=(X1+X2)/2.
        FX3=ID-A1*(VDD-X3-B1*((VDD-X3+VB)**1.5-(VB)**1.5))
        IF(DABS(FX3).LT.1.D-14) GO TO 70
35      IF((FX1*FX3)-0.)72,70,74
74      X1=X3
        GO TO 50
72      X2=X3
        GO TO 50
70      VD1=X3
        GO TO 66
60      ID=ID2
        X1=VP+VB-VB
        X2=0.0
        FX1=ID-A*(X1-B*((X1-VB+VB)**1.5-(VB-VB)**1.5))
```

```
12      R6=-V5/IS
        GO TO 13
11      R6=1./38.7/IS
13      CONTINUE
        IF(VD.LT.0.D0) GO TO 16
        IF((VD-V5+VB).GE.VP) GO TO 14
        ID=A*(VD-B*((VD-V5+VB)**1.5-(VB-V5)**1.5))
        GO TO 8
14      ID=ISAT*(1.-3.*((VB-V5)/VP)+2.*((VB-V5)/VP)**1.5)
8       CONTINUE
        GO TO 17
16      ID=0.D0
17      IF(V5.LT.(-VP+VB)) ID=0.D0
        RETURN
        END
        SUBROUTINE DCFET(A,B,R6,R10,VD1,R4,VDD,VP,VB,ISAT,ISAT1,A1,B1,V3,
       2ID,V5,IS)
C       ------------------------------------------------------------------
C       BISECTION METHOD IS FOR FINDING THE ROOT
C       THIS SUBROUTINE CARIES OUT THE D.C ANALYSIS OF THE
C       CIRCUIT SHOWN IN FIG-5.1
C       ------------------------------------------------------------------
        DOUBLE PRECISION A,B,R10,R6,VD1,R4,VDD,VP,VB,ISAT,V3,ID,V5,X1,X2,
       2X3,FX1,FX2,FX3,IS,A1,B1,ISAT1,ID1,ID2
        CALL PLOT(2000)
        IF(V3.LE.(-5.)) GO TO 1
        IF(V3.EQ.VB) GO TO 2
        IF(V3.LT.(-3.)) GO TO 3
        R6=(V3-VB)/(IS*(DEXP(38.7*(V3-VB))-1.))
        GO TO 5
3       R6=-V3/IS
        GO TO 5
2       R6=1./38.7/IS
5       V5=V3*R6/(R4+R6)
        R10=VB/(IS*(1.-DEXP(38.7*(-VB))))
        ID1=ISAT*(1.-3.*((VB-V5)/VP)+2.*((VB-V5)/VP)**1.5)
        ID2=ISAT1*(1.-3.*(VB/VP)+2.*(VB/VP)**1.5)
        IF(ID1.GT.ID2) GO TO 60
        ID=ID1
        X1=VDD-VP+VB
        X2=VDD
        FX1=ID-A1*(VDD-X1-B1*((VDD-X1+VB)**1.5-(VB)**1.5))
50      X3=(X1+X2)/2.
        FX3=ID-A1*(VDD-X3-B1*((VDD-X3+VB)**1.5-(VB)**1.5))
        IF(DABS(FX3).LT.1.D-14) GO TO 70
35      IF((FX1*FX3)-0.)72,70,74
74      X1=X3
        GO TO 50
72      X2=X3
        GO TO 50
70      VD1=X3
        GO TO 66
60      ID=ID2
        X1=VP+VB-VB
        X2=0.0
        FX1=ID-A*(X1-B*((X1-VB+VB)**1.5-(VP-VB)**1.5))
```

```
C       ELECTRICAL  LENGTH  AND  THE  BASIC  TIME  STEP  DT  SPECFIED
C       VB1 - GATE  BIAS
C       KTM - TOTAL  NO  OF  TIME  STEPS  IN  TRANSIENT  ANALYSIS
C       PA - PULSE  AMPLITUDE  AT  THE  GENERATOR
C       VINC - VOLTAGE  VARIABLES  FOR  TRANSMISSION  LINE  ANALYSIS
C       VREF - VOLTAGE  VARIABLES  FOR  TRANSMISSION  LINE  ANALYSIS
C       VS - VOLTAGE  OF  THE  INPUT  PULSE  AT  THE  GENERATOR
C       ------------------------------------------------------------
        DIMENSION VINC(402,2),VREF(402,2),VS(100),E(305),F(305),C(305),
       2C(10)
        DOUBLE PRECISION ZA,VB1,PA,RL,VINC,VREF,VS,VI,VC,RT,IIN,ICUT,V,VL
       2,A,B,ISAT,IS,DT,TD,R4,VP,VB,D,E,F,C1,CC,L2,C7,LS,V10,C11,R12,C13
        COMMON A,B,ISAT,IS,DT,TD,R4,VP,VB,C1,CC,L2,C7,LS,V10,C11,R12,C13
C ***   MESFET  DATA  TO  BE  SPECIFIED
C       ********************************
        READ(5,100)A,B,ISAT,IS,DT,RL,C7
        READ(5,100)RT,VP,C1,VB,CC,L2,LS
        C11=4.*C1
        C13=C1
        R12=.CC.
        V10=10.
        VC=0.0
C       ********************************
C ***   CONTROLLED  PARAMETERS
C       ********************************
        R4=10.DC
        ZA=50.DO
        TD=5.D-12
C       ********************************
        WRITE(6,311)
        WRITE(6,308)
 308    FORMAT(34X,*CALCULATION FOR NEGATIVE INPUT PULSE*)
        WRITE(6,309)
 309    FORMAT(32X,41(1H-),/)
        READ(5,310)KTM,LA
 310    FORMAT(2(I3))
        PI=1.DO4
        WRITE(6,311)
 311    FORMAT(/,17X,75(1H-),/)
        WRITE(6,101)A,B,ISAT,IS,DT,RL,C7
        WRITE(6,101)RT,VP,C1,VB,CC,L2,LS
        WRITE(6,311)
 100    FORMAT(7D11.4)
 101    FORMAT(/,15X,7(2X,D11.4))
        WRITE(6,311)
        WRITE(6,312)TD,ZA,R4
 312    FORMAT(20X,*TD=*,D11.4,6X,*ZA =*,D11.4,6X,*R4=*,D11.4)
        WRITE(6,311)
        K1=1
        DO 4 L=1,2
        READ(5,306)VB1
 306     FORMAT(D11.4)
        E(L)=VB1
        NS=LA+1
        PA=-10.
        RL=50.DO
```

```
C         INITIAL  VANC I
      DO 1 J=1,NS
      VINC(J,1)=0.DO
    1 VREF(J,1)=0.DO
C       INPUT PULSE
      DO 2 J=1,80
    2 VS(J)=FLOAT(J)*PA/80.DO
      DO 3 J=81,160
    3 VS(J)=PA*(1.DO-(FLOAT(J)-80.)/80.DO)
      DO 41 J=161,KTM
   41 VS(J)=0.DO
C    TRANSIENT CALCULATIONS
      DO 4 K=1,KTM
      VINC(1,2)=VS(K)
      VREF(1,2)=VREF(2,1)
      DO 5 J=2,LA
      VINC(J,2)=VINC(J-1,1)
    5 VREF(J,2)=VREF(J+1,1)
      VINC(NS,2)=VINC(LA,1)
      V2=VINC(NS,2)
      CALL FET(V1,VG,K,IIN,IOUT,ZA,RL,VB1,RT)
      VREF(NS,2)=VINC(NS,2)-2.DO*IIN*ZA
      V=(VINC(1,2)+VREF(1,2))/2.DO
      VL=IOUT*RL
      DO 6 J=1,NS
      VINC(J,1)=VINC(J,2)
    6 VREF(J,1)=VREF(J,2)
      TIME=FLOAT(K)*0.125
      IF(TIME.LT.25.)GO TO 4
      IF(K.EQ.(K/8)*8) GO TO 7
      GO TO 4
7     E(K1)=V
      F(K1)=VL
      C(K1)=TIME
      K1=K1+1
4     CONTINUE
14    CONTINUE
      WRITE(6,300) D(1),D(2),D(3)
300   FORMAT(3(3X,*VALUE OF VG *,D11.4,13X))
      WRITE(6,301)
301   FORMAT(1X,3(34(1H-),7X))
      WRITE(6,302)
302   FORMAT(3(2X,*VOL.AT.INP*,3X,*VOL.AT.LOAD*,4X,*TIME *,7X))
303   FORMAT(3(4X,*IN VOLTS*,6X,*IN VOLTS*,6X,*SEC*,7X))
      WRITE(6,304)
304   FORMAT(3(3X,11(1H-),3X,11(1H-),4X,3(1H-),7X))
      DO 45 I=1,76
      N1=I+76
      M1=I+1+82
      WRITE(6,305)E(I),F(I),C(I),E(N1),F(N1),C(N1),E(M1),F(M1),C(N1)
305   FORMAT(/,3(1X,D12.5,2X,D12.5,3X,F7.2,6X))
45    CONTINUE
      STOP
      END
      SUBROUTINE FET(V1,VG,K,IIN,IOUT,ZI,ZZ,V3,RL)
C     ---------------------------------------------------------------
```

```
C      THIS  SUBROUTINE  CARIES  OUT  THE  TRANSIENT  ANALYSIS  OF  THE
C      AMPLIFIER  IN  SOURCE  FOLLOWER  CONFIGURATION.
C      NOTATIONS  REMAIN  THE  SAME  AS  SHOWN  IN  THE  FIG -6.1
C      ------------------------------------------------------------------
       DOUBLE PRECISION VI,VO,IIN,ICUT,Z1,Z2,VB,RL,DT,TD,C1,VB,IS,VP,CO,
      2A,B,ISAT,RLP,L2,R4,CT,L9,V10,C11,R12,C13,VK,R6,V1,I2,I13,I1,I5,I7,
      3I11,V2,V9,V11,I9,IC,I12,V13,IK,V5,C5,V7,I8,VD,VL
       COMMON A,B,ISAT,IS,DT,TD,R4,VP,VB,C1,CO,L2,C7,L9,V10,C11,R12,C13
       DIMENSION I8(1000)
       RLP=RL/(RL+Z2)
       KC=(TD/DT)+1.
C***   INITIAL  BIAS  CONDITIONS
       IF(K.GT.1) GO TO 1
       CALL DRAIN(VP,R12,ISAT,IS,R4,VL,ID,R6,VB,VB)
    5  CONTINUE
       VB=-VL
   73  V1=-VB
   72  CONTINUE
       V11=V10
       I9=-IC
       I2=-VB/R4
       V13=VB+I2*R4-VB
       V7=V13+I2*R4-VB
       C5=CO/(1.-VB/VB)**0.5
       DO 71 J=1,KC
    71 I8(J)=ID
       GO TO 8
C***   TRANSIENT  ANALYSIS
    1  CONTINUE
       IF(VB.GE.VB) GO TO 9
       C5=CO/(1.-VB/VB)**0.5
       GO TO 10
    9  C5=CO/(1.-VB/(VB-1.D-7))**0.5
   10  IF(VB.EQ.VB) GO TO 11
       IF(VB.LT.(-3.)) GO TO 12
       R6=(VB-VB)/(IS*(DEXP(36.7*(VB-VB))-1.))
   12  R6=-VB/IS
       GO TO 13
   11  R6=1.D0/36.7DO/IS
   13  CONTINUE
       VD=V10+V9
       IF((VD-VB+VB).GT.VP) GO TO 14
       ID=A*(VD-B*((VD-VB+VB)**1.5-(VB-VB)**1.5))
       GO TO 8
   14  ID=ISAT*(1.-3.*((VB-VB)/VP)+2.*((VB-VB)/VP)**1.5)
    8  CONTINUE
       IF(VD.LT.(-VP+VB)) ID=0.0
       K1=KC-1
       DO 81 J=1,K1
       KC1=KC-J+1
       KC2=KC-J
   81  I8(KC1)=I8(KC2)
       I8(1)=ID
       I13=(V7+V13)-(VB+V13+VD*RLP))/(Z2*RLP)
       I2=(VB-V13+I2*R4-V7-V13)/(Z1+R4)
       I7=I1-I2+I8(KC)-(V7+V13-VB+I13*R12)/R12
```

```
      IF(R6.LE.0.00) GO TO 15
      I5=I1-(I2+I7+V5/R6)
      GO TO 16
   15 I5=0.00
   16 CONTINUE
      I11=I7-(I9+I8(KD))
      V2=V1-(Z1*I1+V1+V3)
      V9=V11-V10
  510 V1=V1+I1*(DT/C1)
      V13=V13+I13*(DT/C13)
      V7=V7+I7*(DT/C7)
      V11=V11+I11*(DT/C11)
      V5=V5+I5*(DT/C5)
      I2=I2+V2*(DT/L2)
      I9=I9+V5*(DT/L5)
   19 IF(V5.GT.VE)  GO TO 17
      GO TO 18
   17 V5=VE-1.0-7
   18 CONTINUE
C***  I IN AND IOUT RETURN TO THE MAIN PROGRAM
      I=M1
      IOUT=I13*RLF-(VG/(Z2+RL))
      RETURN
      END
      SUBROUTINE CRAIN(VB,R,ISAT,IS,R4,VL,IC,R6,V8,VB)
C     ------------------------------------------------------------------
C     THIS  SUBROUTINE  CARIES  OUT  THE  D.C  ANALYSIS  OF  THE
C     CIRCUIT  SHOWN  IN  FIG-6.1
C     BISECTION  METHOD  IS  FOR  FINDING  THE  ROOT
C     ------------------------------------------------------------------
      DOUBLE PRECISION V5,X,Y,FA,FB,X1,X2,X3,FX1,FX2,FX3,IC,ISAT,VB,VP,R
     I,IS,R4,VL,VM,VK,R6,V3
      V5=-V3
      IF(V5.GE.5.) GO TO 16
      X=25.7D-3
      Y=20.0-3
      FA=X-ISAT*(1.-3.*((V5+VB+X*R)/VP)+2.*((V5+VB+X*R)/VP)**1.5)
      DO 1 ITER=1,30
      FB=Y-ISAT*(1.-3.*((V5+VB+Y*R)/VP)+2.*((V5+VB+Y*R)/VP)**1.5)
      IF((FB*FA)-0.)3,26,26
   26 Y=Y+0.0001
    1 CONTINUE
    3 X1=X
      X2=Y
      FX2=FB
      FX1=FA
      X3=(X1+X2)/2.
      VK=V5+X3*R
      IF(VK.EQ.VP) GO TO 11
      IF(VK.GT.2.) GO TO 12
      R6=(-VK-VB)/(IS*(DEXP(38.7*(-VK-VB))-1.))
      GO TO 13
   12 R6=VK/IS
      GO TO 13
   11 R6=1./38.7/IS
   13 CONTINUE
```

```
      GC TC 17
50    IF(VM.EQ.VP) GC TC 14
      IF(VM.GT.3.) GC TC 18
      R6=(-VM-VB)/(IS*(DEXP(38.7*(-VM-VB))-1.))
      GC TC 16
15    R6=VM/IS
      GC TC 16
14    R6=1./38.7/IS
16    CCNTINUE
      X3=(X2+X1)/2.
17    VM=R6*(VS+X3*R)/(R6+R4+R)
      FX3=X3-ISAT*(1.-3.*((VM+VB)/VP)+2.*((VM+VB)/VP)**1.5)
      IF(DABS(FX3)-1.D-14)71,71,355
355   IF((FX1*FX3)-0.)70,71,72
 72   X1=X3
      GC TC 50
70    X2=X3
      GC TC 50
 71   WRITE(6,313)FX3,X3
313   FORMAT(2(2X,D11.4))
      ID=X3
      VL=VM
      GC TC 19
  18  ID=0.0
      R4=VS/IS
      VL=VS
19    CCNTINUE
      RETURN
      END
C     DATA  CARDS
C
C
C
C
C
C
C
C     ---------------------------------------------------------------------------------
C
C
C
C
C
C
C
C
C
C
C
C
C
C
C------------------------------------------------------------------------------------------
C     THIS  PRCGRAM  CARRIES  OUT  TRANSIENT  ANALYSIS  OF  CIRCUIT
C     SHCWN  IN  FIG4.3 . SOME  OF  THE  IMPORTANT  NCTATIONS  ARE
C     EXPLAINED  BELOW . THE  MAIN  PROGRAM  CARRIES  MAINLY  THE
C     TRANSIENT  ANALYSIS  OF  TRANSMISSION  LINE .
C     ZA  -  CHARACTERISTICS  IMPEDENCE  OF  INPUT  LINE
C     LA  -  NUMBER  OF  SEGMENTS  IN  IN  INPUT  LINE . IT  DEPENDS
C     ON  THE  ELECTRICAL  LENGTH  AND  THE  BASIC  TIME  STEP  DT
C     SPECIFIED .
C     VB1  -  GATE  BIAS .
```

```
C       KTM  -  TOTAL  NO  OF  TIME  STEPS  IN  TRANSIENT  ANALYSIS  .
C       PA   -  PULSE  AMPLITUDE  AT  THE  GENERATOR  .
C       VINC  -  VOLTAGE  VARIABLE  FOR  TRANSMISSION  LINE  ANALYSIS .
C      VREF   -  VOLTAGE  VARIABLE  FOR  TRANSMISSION  LINE  ANALYSIS .
C       VS   -  VOLTAGE  OF  THE  INPUT  PULSE  AT  THE  GENERATOR  .
C-----------------------------------------------------------------------
      DIMENSION VINC(402,2),VREF(402,2),VS(10(0),E(305),F(305),C(305),
     2D(10)
      DOUBLE PRECISION ZA,VB1,PA,RL,VINC,VREF,VS,RT,IIN,ICLT,V,VL,DT,C1,
     2VB,IS,VP,CO,A,B,C7,LS,V10,C11,TO,R4,V0,VI
      COMMON DT,C1,VB,IS,VP,CO,A,B,ISAT,L2,C7,LS,V10,C11
C ***   MOSFET  DATA  TO  BE  SPECIFIED
C      **********************************
      READ(5,306)DT,C1,VB,IS,VP
      READ(5,306)CO,A,B,ISAT,L2
      READ(5,306)C7,LS,V10,C11,V0
C      **********************************
C ***   CONTROLLED  PARAMETERS
C      **********************************
      TO=5.0-12
      VB1=0.0
      R4=1.0
C      **********************************
      WRITE(6,308)
  308 FORMAT(34X,'CALCULATION FOR NEGATIVE INPUT PULSE')
      WRITE(6,308)
      WRITE(6,309)
  309 FORMAT(32X,41(1H-),/)
      READ(5,310)KTM,LA
  310 FORMAT(2(I3))
      RT=1.004
      WRITE(6,311)
  311 FORMAT(/,17X,75(1H-),/)
      WRITE(6,307)DT,C1,VB,IS,VP
      WRITE(6,307)CO,A,B,ISAT,L2
      WRITE(6,307)C7,LS,V10,C11,V0
  306 FORMAT(5(D11.4))
  307 FORMAT(/,15X,5(4X,D11.4))
      WRITE(6,311)
      WRITE(5,312)ZA,VB1,R4
  312 FORMAT(14X,3(9X,D11.4))
      WRITE(6,311)
      K1=1
      DO 14 L=1,3
      READ(5,101)Z(
  101 FORMAT(D11.4)
      C(L)=ZA
      NS=LA+1
      RL=50.00
C        INITIAL  VAND  I
      DO 1 J=1,NS
      VINC(J,1)=0.00
    1 VREF(J,1)=0.00
C ***   INPUT   PULSE
      PA=-10.
      DO 2 J=1,80
```

```
   2    VS(J)=FLOAT(J)*P1/60.00
        DO 3 J=61,160
   3     VS(J)=P4*(1.00-(FLOAT(J)-60.)/60.00)
        DO 41 J=161,KTN
  41  VS(J)=0.00
C     TRANSIENT CALCULATIONS
        DO 4 K=1,KTN
        VINC(1,2)=VS(K)
        VREF(1,2)=VREF(2,1)
        DO 5 J=2,LA
        VINC(J,2)=VINC(J-1,1)
   5    VREF(J,2)=VREF(J+1,1)
        VINC(NS,2)=VINC(LA,1)
        VI=VINC(NS,2)
        CALL FET(VI,VO,K,IIN,IOUT,ZA,RL,VB1,R1,R4,TD)
        VREF(NS,2)=VIN(NS,2)-2.00*IIN*ZA
        V=(VINC(1,2)+VREF(1,2))/2.00
        VL=IOUT*RL
        DO 6 J=1,NS
        VINC(J,1)=VINC(J,2)
   6    VREF(J,1)=VREF(J,2)
        TIME=FLOAT(K)*0.125
        IF(TIME.LT.25.)GO TO 4
        IF(K.EQ.(K/8)*8) GO TO 7
        GO TO 4
 7      E(K1)=V
        F(K1)=VL
        C(K1)=TIME
        K1=K1+1
   4    CONTINUE
  14    CONTINUE
        WRITE(6,300) D(1),D(2),D(3)
 300    FORMAT(3(5X,*VALUE OF R4 *,D11.4,13X))
        WRITE(6,301)
  301    FORMAT(1X,3(34(1H-),7X))
        WRITE(6,302)
 302    FORMAT(3(1X,*VOL.AT.INP*,3X,*VOL.AT.LOAD*,4X,*TIME*,7X))
        WRITE(6,303)
  303   FORMAT(3(4X,*IN VOLTS*,6X,*IN VOLTS*,6X,*SEC*,7X))
        WRITE(6,304)
 304    FORMAT(3(1X,11(1H-),3X,11(1H-),4X,5(1H-),7X))
        DO 45 I=1,76
        N1=1476
        N1=1+I*2
        WRITE(6,305)E(I),F(I),C(I),E(N1),F(N1),C(N1),E(N1),F(N1),C(N1)
 305    FORMAT(1X,3(1X,D12.5,2X,D12.5,4X,F5.1,7X))
  45    CONTINUE
        STOP
        END
C-------------------------------------------------------------------
C       THIS SUBROUTINE CARRIES THE TRANSIENT ANALYSIS OF MESFET
C       AMPLIFIER IN COMMON SOURCE CONFIGURATION.
C       NOTATION REMAINS THE SAME AS SHOWN IN THE FIG4.1 .
C-------------------------------------------------------------------
        SUBROUTINE FET(VI,VO,K,IIN,IOUT,Z1,Z2,V3,RL,R4,TD)
      DOUBLE PRECISION VINC,VREF,Z1,V3,VS,IIN,IOUT,PA,RL,V1,VO,V,Z2,I1
```

```
     2,ISAT,L2,L9,I2,I7,I8,I11,I5,I9,ID,IS,VP,CO,A,B,RLP,C1,R4,C7,V10
     3,C11,R6,VC,V8,C8,V9,V11,DT,TC,V6,V2,V1,V9
      DIMENSION I8(59)
      COMMON DT,C1,V8,IS,VP,CO,A,B,ISAT,L2,C7,L9,V10,C11
      CALL PLUN(920000)
       RLP=RL/(RL+2.)
       KD=(TD/DT)+1.
       IF(K.GT.1)GO TO 1
C    INITIAL BIAS CONDITIONS
       IF(V8.EQ.V8)GO TO 2
      IF(V8.LT.(-3.DO)) GO TO 3
       R6=(V8-V8)/(IS*(DEXP(38.7DO*(V8-V8))-1.DO))
       GO TO 5
    3  R6=-V8/IS
       GO TO 5
    2  R6=1.DO/38.7DO/IS
    5  CONTINUE
       V5=V8*R6/(R4+R6)
       C5=CO/(1.-V5/V8)**.5
       IF((V10-V5+V8).GE.VP) GO TO 4
       ID=A*(V10-B*((V10-V5+V8)**1.5-(V8-V5)**1.5))
       GO TO 7
C      ID=ISAT*(1.DO-3.DO*((V8-V5)/VP)+2.DO*((V8-V5)/VP)**1.5)
    7  CONTINUE
       DO 71 J=1,KD
   71  I8(J)=ID
       V1=-V8
       I2=-V8/(R4+R6)
       V7=V5-V10
       I9=-ID
       V11=V10
       GO TO 8
C    TRANSIENT ANALYSIS
    1  CONTINUE
       IF(V5.GE.V8)GO TO 9
       C5=CO/(1.DO-V5/V8)**.5
       GO TO 10
    9  C5=CO/(1.DO-V8/(V8-1.D-7))**.5
   10  IF(V5.EQ.V8)GO TO 11
       IF(V5.LT.(-3.DO)) GO TO 12
       R6=(V5-V8)/(IS*(DEXP(38.7DO*(V5-V8))-1.DO))
       GO TO 13
   12  R6=-V5/IS
       GO TO 13
   11  R6=1.DO/38.7DO/IS
   13  CONTINUE
       VC=V10+V9
       IF((VC-V8+V8).GE.VP)GO TO 14
       ID=A*(VC-B*((VC-V5+V8)**1.5-(V8-V5)**1.5))
       GO TO 8
   14  ID=ISAT*(1.DO-3.DO*((V8-V5)/VP)+2.DO*((V8-V5)/VP)**1.5)
    8  CONTINUE
       IF(V8.LT.(-VP+V8)) ID=0.DO
       L=KD-1
       DO 81 J=1,L
       KD2=KD-J+1
```

```
      KC2=KC-2
   81 IS(KC1)=IS(KC2)
      IS(1)=IC
      I11=(V5-V11-VC*RLP+V1)/(Z2+RLP)
      I7=IS(KC)+I9+I11
      I1=(V1-V11+I2*R4-V5)/(Z1+R4)
      V2=V -Z1*I1-V1+V5
      V5=V11+V5*RLP+Z2*I11*RLP-V1C
      IF(R6.LE.0.0)GO TO 15
      I5=I1-I2-V5/R6-I7
      GO TO 16
   15 I5=0.0C
   16 CONTINUE
      V11=V11+I11*(DT/C11)
      V1=V1+I1*(DT/C1)
      I9=I9+V9*(DT/L9)
       V7=V7+I7*(DT/C7)
      I2=I2+V2*(DT/L2)
      V5=V5+I5*(DT/C5)
   19 IF(V5.GT.VC)GO TO 17
      GO TO 18
   17 VC=VC+1.0-7
   18 CONTINUE
C     IIN IOUT RETURNED TO THE MAIN PROGRAM-
      IIN=I5
      IOUT=I11*RLP-(V0/(Z2*RL))
      RETURN
      END
C     DATA  CARDS
```

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